120-mΩ, Quad-Channel, High-Side Switch

Features

- Quad channel high-side switch with complete diagnosis and protection
  - 120 mΩ $R_{DS(on)}$ per channel
  - Open-drain digital output: DIO74H120A
  - Current sense analog output: DIO74H120B
- Wide input voltage range: 3.7 to 40 V
- Less than 300 nA ultra low standby current
- Diagnostics:
  - Overcurrent detection
  - Open load detection
  - Short circuit to ground and battery detection
  - Global fault with fast interrupt
- Protection:
  - Absolute temperature limitation with latch off option
  - Thermal swing protection
  - Inductive load negative voltage clamp with optimized slew rate
  - Undervoltage shutdown
  - Loss of ground protection
  - Loss of battery protection
  - High accurate adjustable current limit with external resistor, ±20% at > 500 mA load

Package Information

Part Number	Package	Body Size
DIO74H120	EP-TSSOP28	9.7 mm × 4.4 mm
	QFN-28	4.0 mm × 5.0 mm

Applications

- Industrial PLC system
- Digital output modules
- Solenoid or valve drive
- Standalone remote I/O

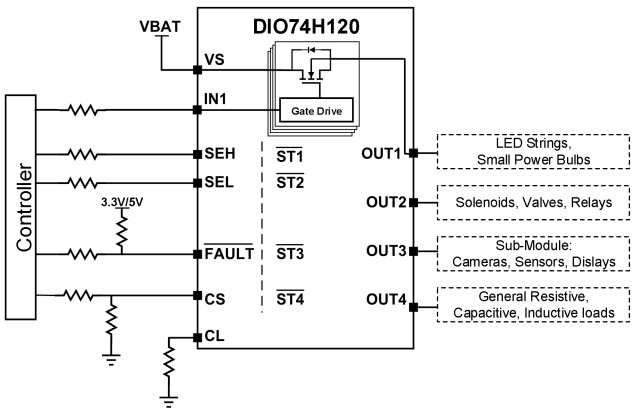
Description

The DIO74H120 is a fully protected, quad-channel, smart, high-side driver and housed in EP-TSSOP28 and QFN-28 packages. Every channel integrates a 120 mΩ high-voltage NMOS power FET to drive the industrial grounded loads.

The DIO74H120 offers complete protection functions. The device enables to adjust internal current limit by using external resistors, which can limit the inrush or overload current. With the current limit function, its internally integrated comprehensive overtemperature protection scheme can greatly improve the reliability of the system.

High-accuracy current sense enables to monitor the current flowing through the switch in real time so as to provide a more accurate diagnosis without further external calibration.

Simplified Schematic



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Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO74H120AXT28	DIOHA2A	3	Green	-40°C to 125°C	EP-TSSOP28	Tape & Reel, 2500
DIO74H120BXT28	DIOHA2B	3	Green	-40°C to 125°C	EP-TSSOP28	Tape & Reel, 2500
DIO74H120AEN28	DIOHA2A	3	Green	-40°C to 125°C	QFN4×5-28	Tape & Reel, 3000
DIO74H120BEN28	DIOHA2B	3	Green	-40°C to 125°C	QFN4×5-28	Tape & Reel, 3000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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Table of Contents

1. Pin Assignment and Functions 1
2. Absolute Maximum Ratings 3
3. Recommended Operating Conditions 4
4. ESD Ratings 4
5. Thermal Considerations 4
6. Electrical Characteristics 5
7. Typical Characteristic 10
8. Block Diagram 12
9. Function Description 13
    9.1. Current sense 13
    9.2. Adjustable current limit 13
    9.3. Inductive-load switching-off clamp 14
    9.4. Fault detection and reporting 14
    9.5. Full diagnostics 16
    9.6. Full protection 17
    9.7. Device function modes 19
10. Application Information 20
    10.1. Typical application 20
    10.2. Detailed design 21
    10.3. Application curves 21
11. Layout Guidelines 21
12. Physical Dimensions 22
12.1. EP-TSSOP28 22
12.2. QFN4×5-28 23

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List of Figures

Figure 1. EP-TSSOP28 - DIO74H120A (Top view) 1
Figure 2. EP-TSSOP28 - DIO74H120B (Top view) 1
Figure 3. QFN4×5-28 - DIO74H120A (Top view) 1
Figure 4. QFN4×5-28 - DIO74H120B (Top view) 1
Figure 3. Output delay related time parameters 8
Figure 4. CS delay related time parameters 9
Figure 5. Open-load blanking time 9
Figure 6. Multi-sense transition related time parameters 9
Figure 7. $I_{(op)}$ vs. V_{VS} 10
Figure 8. $I_{(op)}$ vs. Temperature 10
Figure 9. $I_{(off, diag)}$ vs. V_{VS} 10
Figure 10. $I_{(off, diag)}$ vs. Temperature 10
Figure 11. $R_{DS(on)}$ vs. Temperature 10
Figure 12. Current sense ratio vs. I_{OUT} 10
Figure 13. Turn on 11
Figure 14. Turn off 11
Figure 15. Driving a capacitive load with adjustable current limit 11
Figure 16. Driving a capacitive load, expanded waveform 11
Figure 17. Inductive load switching-off waveform 11
Figure 18. PWM signal driving 11
Figure 19. Current-sense output-voltage curve 13
Figure 20 . Protection with external circuitry 14
Figure 21. Protection for loss of power supply (type 1) 17
Figure 22. Protection for loss of power supply (type 2) 17
Figure 23. Reverse-current external protection (type 1) 18
Figure 24. Reverse-current external protection (type 2) 18
Figure 25. Working modes 19
Figure 26. Typical applicaiton 20

List of Tables

Table 1. Diagnosis configuration 15
Table 2. Fault table 15
Table 3. Recommended external components 20

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1. Pin Assignment and Functions

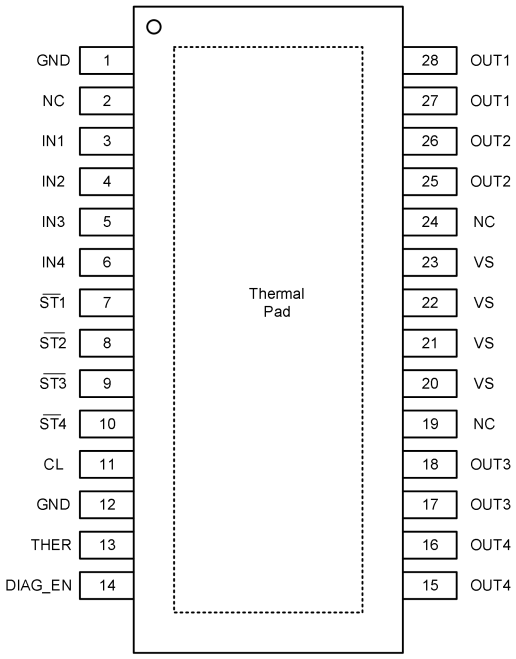

Figure 1. EP-TSSOP28 - DIO74H120A (Top view)

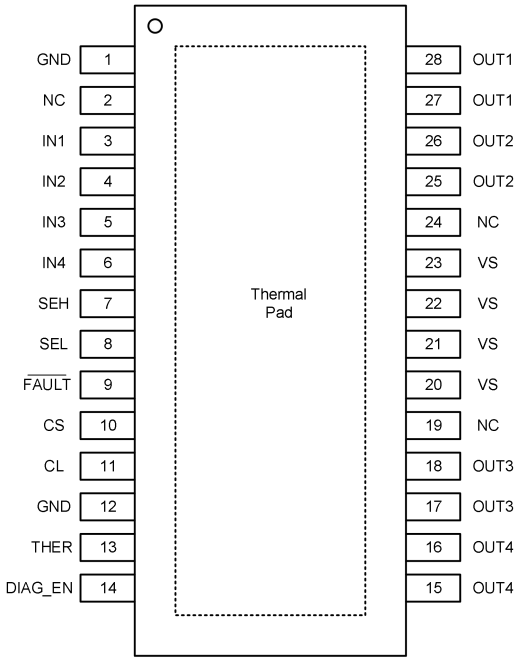

Figure 2. EP-TSSOP28 - DIO74H120B (Top view)

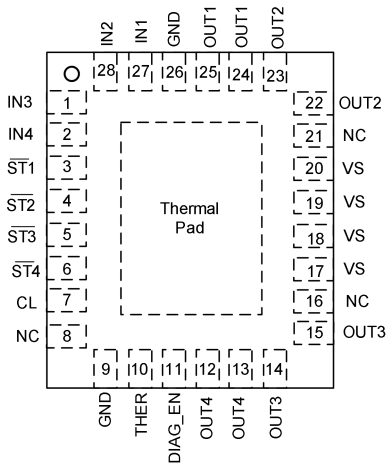

Figure 3. QFN4×5-28 - DIO74H120A (Top view)

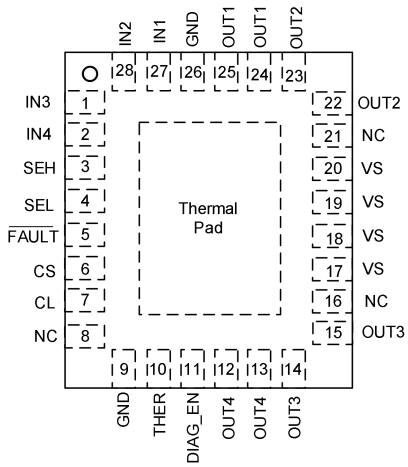

Figure 4. QFN4×5-28 - DIO74H120B (Top view)

Pin Name	I/O	Description
GND		Ground pin
NC		No internal connection
INx	I	Input control for channel X activation;internal pulldown
$\overline{STx}$	O	Open-drain diagnostic status output for channel x
SEH	I	CS channel-selection high bit; internal pulldown
SEL	I	CS channel-selection low bit; internal pulldown
$\overline{FAULT}$	O	Global fault report with open-drain structure, ORed logic for quad-channel fault conditions
CS	O	Current-sense output

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CL	O	Adjustable current limit. Connect to device GND if external current limit is not used
THER	I	Thermal shutdown behavior control, latch off or auto-retry; internal pulldown
DIAG_EN	I	Enable-disable pin for diagnostics; internal pulldown
OUTx	O	Output of the channel x high side-switch, connected to the load
VS	I	Power supply
Thermal pad	-	Connect to device GND or leave floating. Recommend to connect to GND to improve the thermal performance

Note:

(1) x = 1, 2, 3, 4.

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2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
	Supply voltage, t < 400 ms		48	V
	Reverse polarity voltage (1)	-36		V
	Current on GND pin, t < 400 ms	-100	250	mA
	Voltage on INx, DIAG_EN, SEL, SEH, and THER pins	-0.3	7	V
	Current on INx, DIAG_EN, SEL, SEH, and THER pins	-10		mA
	Voltage on $\overline{STx}$ or $\overline{FAULT}$ pins	-0.3	7	V
	Current on $\overline{STx}$ or $\overline{FAULT}$ pins	-30	10	mA
	Voltage on CS pin	-2.7	7	V
	Current on CS pin		30	mA
	Voltage on CL pin	-0.3	7	V
	Current on CL pin		6	mA
	Inductive load switch-off energy dissipation, single pulse, single channel (2)		40	mJ
T_J	Operating junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

Note:

(1) Reverse polarity condition: t < 60 s, reverse current < $I_{R(2)}$, V_{INx} = 0 V, all channels reverse, GND pin 1-kΩ resistor in parallel with diode.

(2) Test condition: V_{VS} = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2 × 70-µm Cu, 2 x 35-µm Cu. 600 mm^2 thermal pad copper area.

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3. Recommended Operating Conditions

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_{VS}	Supply operating voltage	4.2 to 40	V
	Voltage on INx, DIAG EN, SEL, SEH, and THER pins	0 to 5	V
	Voltage on $\overline{STx}$ and $\overline{FAULT}$ pins	0 to 5	V
	Nominal DC load current	0 to 2.5	A
T_A	Operating ambient temperature range	-40 to 125	°C

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Metric	Value	Unit
HBM	Human-body model. JEDEC JS-001	±2000	V
CDM	Charged-device model. JEDEC JS-002	±1000	V

5. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Metric		Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	EP-TSSOP28	32.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		21.4	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		4.4	

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6. Electrical Characteristics

5 V < V_{VS} < 40 V, −40°C < T_J < 150°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Operating voltage						
$V_{VS(nom)}$	Nominal operating voltage		4.2		40	V
$V_{VS(uvr)}$	Undervoltage turn on	V_{VS} rises up	3.5	3.7	4.2	V
$V_{VS(uvf)}$	Undervoltage shutdown	V_{VS} falls down	3.0	3.2	3.7	V
$V_{(uv,hys)}$	Undervoltage shutdown, hysteresis			0.5		V
Operating current						
$I_{(op)}$	Nominal operating current	V_{VS} = 13.5 V, V_{INx} = 5 V, V_{DIAG_EN} = 0 V, I_{OUTx} = 0.5 A, R_{CL} = 1 kΩ, all channels on		5	7	mA
$I_{(off)}$	Standby current	V_{VS} = 13.5 V, V_{INx} = V_{DIAG_EN} = V_{CS} = V_{CL} = V_{OUTx} = THER = 0 V, T_J = 25°C			0.3	μA
		V_{VS} = 13.5 V, V_{INx} = V_{DIAG_EN} = V_{CS} = V_{CL} = V_{OUTx} = THER = 0 V, T_J = 125°C			5	μA
$I_{(off,diag)}$	Standby current with diagnostic enabled	V_{VS} = 13.5 V, V_{INx} = 0 V, V_{DIAG_EN} = 5 V, $V_{VS-VOUTx}$ > $V_{(ol,off)}$, not in open-load mode		1.5	3	mA
$t_{(off,diag)}$	Standby mode deglitch time	IN from high to low, if deglitch time > $t_{(off,deg)}$, the device enters into standby mode.	10	12.5	15	ms
$I_{lkg(out)}$	Output leakage current in off-state	V_{VS} = 13.5 V, V_{INx} = V_{DIAG_EN} = V_{OUTx} = 0			3	μA
Power stage						
$R_{DS(on)}$	On-state resistance	V_{VS} ≥ 3.5 V, T_J = 25°C		120		mΩ
		V_{VS} ≥ 3.5 V, T_J = 150°C			220	mΩ
$I_{CL(int)}$	Internal current limit	Internal current limit value, CL pin connected to GND	8		14	A
$I_{CL(TSD)}$ (2)	Current limit during thermal shutdown	Internal current limit value under thermal shutdown		6.5		A
		External current limit value under thermal shutdown. The percentage of the external current limit setting value		65		%

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$V_{DS(clamp)}$	Drain-to-source internal clamp voltage		50	60	70	V
Output diode						
V_F	Drain−source diode voltage	IN = 0, I_{OUTx} = −0.15 A.	0.3	0.7	0.9	V
$I_{R(1)}$, $I_{R(2)}$ (2)	Continuous reverse current from source to drain	t < 60 s, V_{INx} = 0 V, T_J = 25°C, single channel reversed, short-to-battery condition		2.5		A
		t < 60 s, V_{INx} = 0 V, GND pin 1-kΩ resistor in parallel with diode. T_J = 25°C. Reverse-polarity condition, all channels reversed		2		A
Logic input (INx, DIAG_EN, SEL, SEH, THER)						
V_{IH}	Logic high-level voltage		2			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{(logic,pd)}$	Logic-pin pulldown resistor	INx, SEL, SEH, V_{INx} = V_{SEL} = V_{SEH} = 5 V	250	350	450	kΩ
		DIAG_EN, THER, V_{VS} = V_{DIAG_EN} = V_{THER} = 5 V	75	150	225	kΩ
Diagnostics						
$I_{lkg(GND_loss)}$	Output leakage current under GND loss condition				30	µA
$V_{(ol,off)}$	Open-load detection threshold	IN = 0 V, when V_{VS} – V_{OUTx} < $t_{(ol,off)}$, duration longer than $t_{(ol,off)}$, then open load is detected, off state	1.5			V
$I_{(ol,off)}$	Off-state output sink current	V_{INx} = 0 V, V_{DIAG_EN} = 5 V, V_{VS} = V_{OUTx} = 13.5 V, T_J =125°C, open load	-75			µA
$t_{d(ol,off)}$	Open-load detection threshold deglitch time	IN = 0 V, when V_{VS} – V_{OUTx} < $V_{(ol,off)}$, duration longer than $t_{(ol,off)}$, then open load is detected, off state	300	550	800	µs
$V_{OL(STx)}$	Status low-output voltage	I_{STx} = 2 mA, DIO74H120A only			0.2	V
$V_{OL(FAULT)}$	Fault low-output voltage	I_{FAULT} = 2 mA, DIO74H120B only			0.2	V
$t_{CL(deg)}$ (2)	Deglitch time when current limit occurs	V_{INx} = V_{DIAG_EN} = 5 V, the deglitch time from current limit toggling to FAULT, STx, CS report.	80	125	180	µs
T_{SD}	Thermal shutdown threshold		155	170		°C
$T_{SD,rst}$	Thermal shutdown status reset threshold			140		°C
T_{SW} (2)	Thermal swing shutdown threshold			60		°C

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T_{HYS}	Hysteresis for resetting the thermal shutdown or thermal swing (1)			25		°C
Current sense (for DIO74H120B) and current limit						
$K_{(CS)}$	Current-sense ratio			300		
$K_{(CL)}$	Current-limit ratio			3000		
$V_{CL(th)}$	Current limit internal threshold			0.67		V
$dK_{(CS)}/K_{(CS)}$	Current-sense accuracy, ($I_{CS} \times K_{(CS)} - I_{OUTx}$) / I_{OUTx} × 100	V_{VS} = 13.5 V, I_{OUTx} ≥ 5 mA	-30		30	%
		V_{VS} = 13.5 V, I_{OUTx} ≥ 25 mA	-10		10	%
		V_{VS} = 13.5 V, I_{OUTx} ≥ 50 mA	-8		8	%
		V_{VS} = 13.5 V, I_{OUTx} ≥ 100 mA	-4		4	%
		V_{VS} = 13.5 V, I_{OUTx} ≥ 0.5 A	-3		3	%
$dK_{(CL)}$ / $K_{(CL)}$	External current limit accuracy(1) ($I_{OUTx} - I_{CL} \times K_{(CL)}$) × 100 / ($I_{CL} \times K_{(CL)}$)	V_{VS} = 13.5 V, $I_{(limit)}$ ≥ 0.25 A	-35		35	%
		V_{VS} = 13.5 V, 0.5 A ≤ $I_{(limit)}$ ≤ 7 A	-20		20	%
$V_{CS(lin)}$	Current-sense voltage linear range	V_{VS} ≥ 6.5 V	0		4	V
		5 V ≤ V_{VS} < 6.5 V	0		V_{VS} - 2.5	V
$I_{OUTx(lin)}$ (2)	Output-current linear range	V_{VS} ≥ 6.5 V, $V_{CS(lin)}$ ≤ 4 V	0		2.5	A
		5 V ≤ V_{VS} < 6.5 V, $V_{CS(lin)}$ ≤ V_{VS} - 2.5 V	0		2.5	A
$V_{CS(H)}$	Current-sense pin output voltage	V_{VS} ≥ 7 V, fault mode	4.5		6.5	V
		5 V ≤ V_{VS} < 7 V, fault mode	Min (V_{VS} -2 or 4.5)		6.5	
$I_{CS(H)}$	Current-sense pin output current	V_{CS} = 4.5 V, V_{VS} = 13.5 V	15	18		mA
$I_{lkg(CS)}$	Current-sense leakage current in disabled mode	V_{DIAG_EN} = 0 V, T_J = 125ºC			0.5	μA
Switching						
$t_{d(on)}$	Delay time, V_{OUTx} 10% after VINx↑	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, IN rising edge to 10% of V_{OUTx}	20	50	90	μs
$t_{d(off)}$	Delay time, V_{OUTx} 90% after VINx↓	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, IN falling edge to 90% of V_{OUTx}	20	50	90	μs
dV/dt(on)	Turn-on slew rate	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, V_{OUTx} from 10% to 90%	0.1	0.25	0.55	V/μs
dV/dt(off)	Turn-off slew rate	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, V_{OUTx} from 90% to 10%	0.1	0.25	0.55	V/μs

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$t_{d(match)}$	$t_{d(rise)} - t_{d(fall)}$	V_{VS} = 13.5 V, I_L = 0.5 A. $t_{d(rise)}$ is the IN rising edge to V_{OUTx} = 90%. $t_{d(fall)}$ is the IN falling edge to V_{OUTx} = 10%	-100		100	μs
Current-sense						
$t_{CS(off1)}$	CS settling time from DIAG_EN disabled	V_{VS} = 13.5 V, V_{INx} = 5 V, I_{OUTx} = 0.5 A. current limit = 2 A. DIAG_EN falling edge to 10% of V_{CS}			20	μs
$t_{CS(on1)}$	CS settling time from DIAG_EN enabled	V_{VS} = 13.5 V, V_{INx} = 5 V, I_{OUTx} = 0.5 A. current limit is 2 A. DIAG_EN rising edge to 90% of V_{CS}			20	μs
$t_{CS(off2)}$	CS settling time from IN falling edge	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A. current limit = 2 A. IN falling edge to 10% of V_{CS}	20		100	μs
$t_{CS(on2)}$	CS settling time from IN rising edge	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A. current limit = 2 A. IN rising edge to 90% of V_{CS}	50		180	μs
t_{SEx}	Multi-sense transition delay from channel to channel	V_{DIAG_EN} = 5 V, current sense output delay when multi-sense pins SEL and SEH transition from channel to channel			50	μs

Note:

(1) External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting.

(2) Guaranteed by design.

(3) Specifications subject to change without notice.

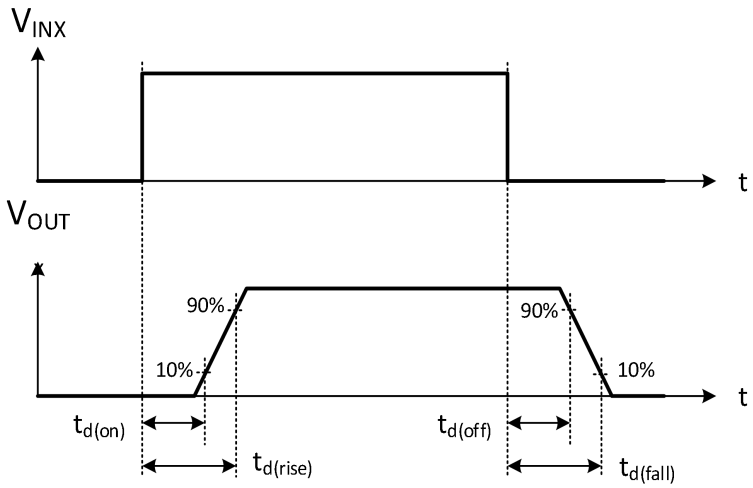

Figure 3. Output delay related time parameters

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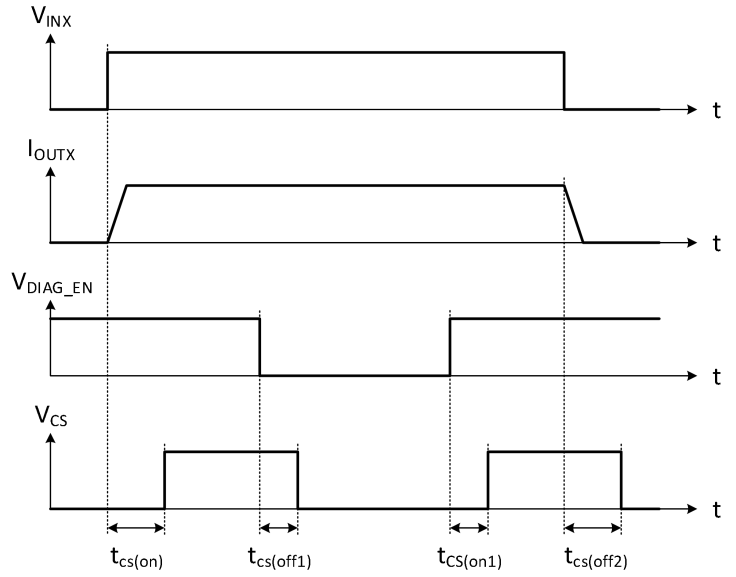

Figure 4. CS delay related time parameters

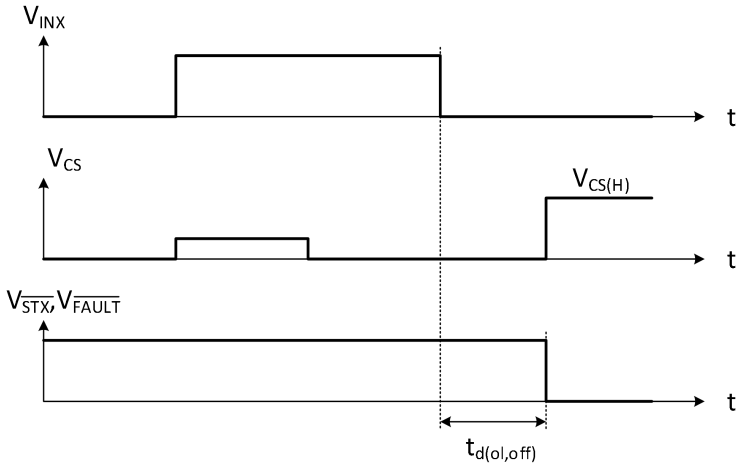

Figure 5. Open-load blanking time

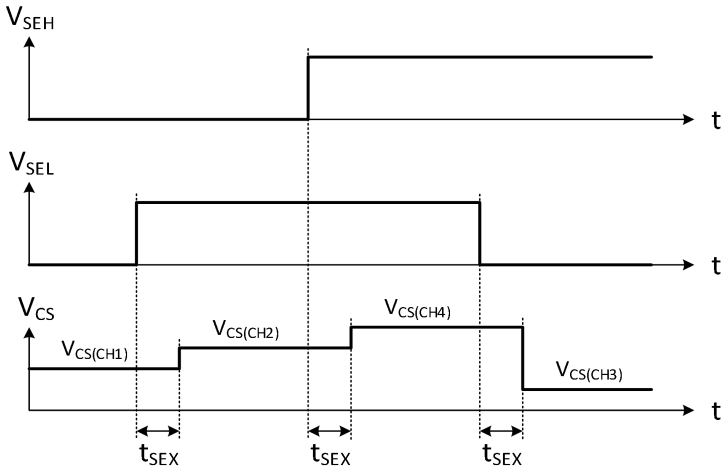

Figure 6. Multi-sense transition related time parameters

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7. Typical Characteristic

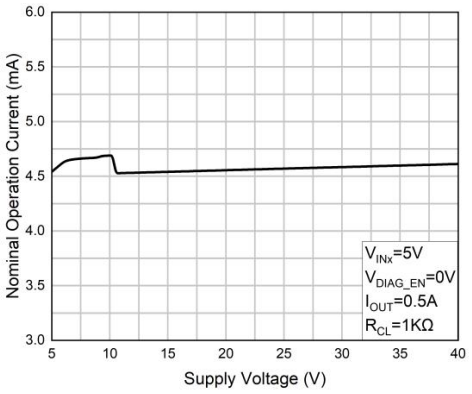

Figure 7. $I_{(op)}$ vs. V_{VS}

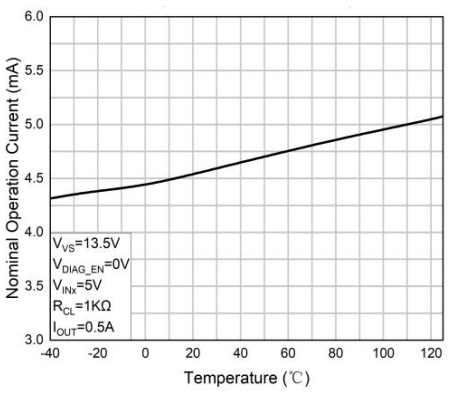

Figure 8. $I_{(op)}$ vs. Temperature

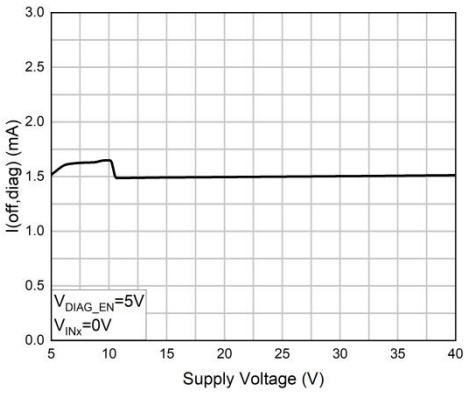

Figure 9. $I_{(off, diag)}$ vs. V_{VS}

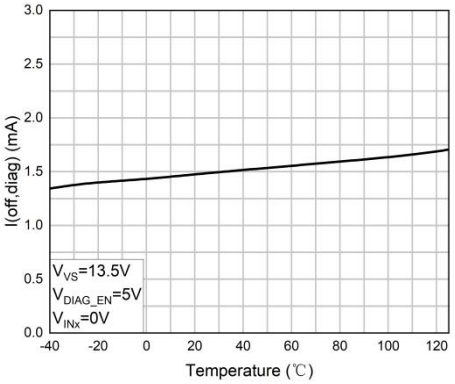

Figure 10. $I_{(off, diag)}$ vs. Temperature

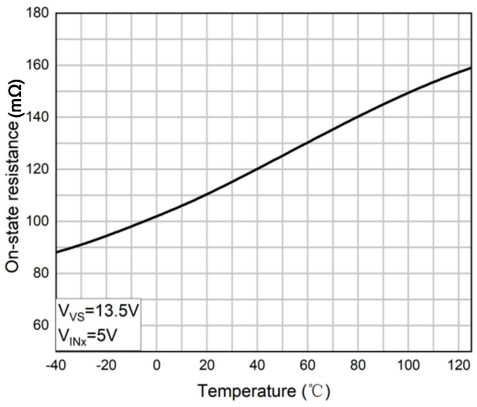

Figure 11. $R_{DS(on)}$ vs. Temperature

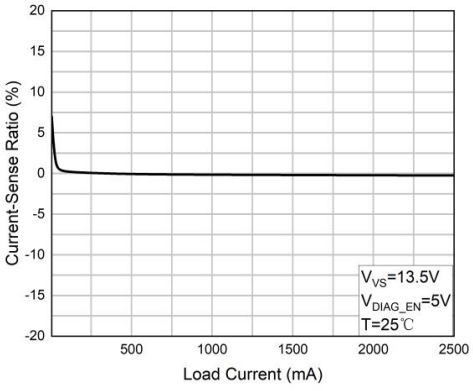

Figure 12. Current sense ratio vs. I_{OUT}

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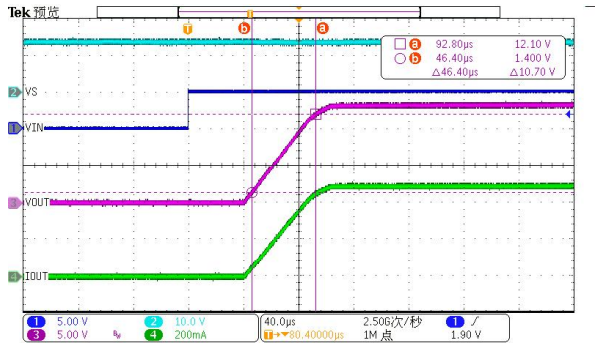
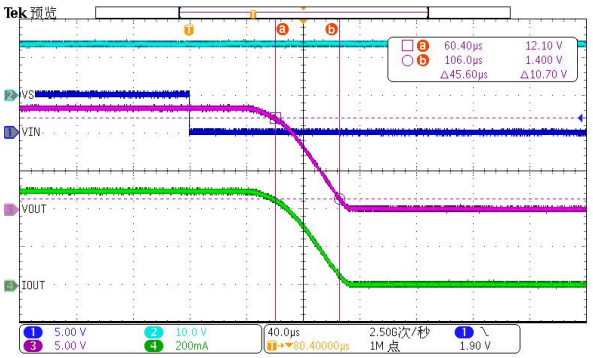


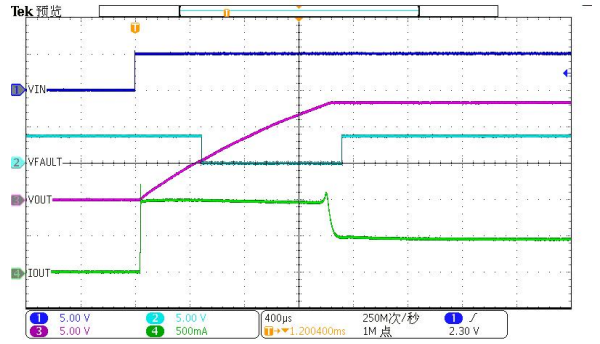
V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A

Figure 13. Turn on



V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A

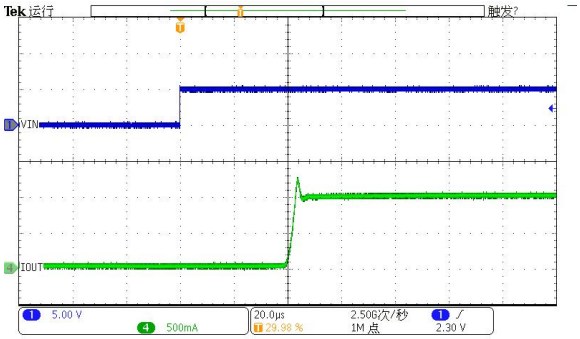
Figure 14. Turn off



V_{VS} = 13.5 V, current limit = 1 A, I_{OUTx} = 0.5 A, C_{Load} = 82 µF

Figure 15. Driving a capacitive load

with adjustable current limit



V_{VS} = 13.5 V, current limit = 1 A, I_{OUTx} = 0.5 A, C_{Load} = 82 µF

Figure 16. Driving a capacitive load, expanded waveform

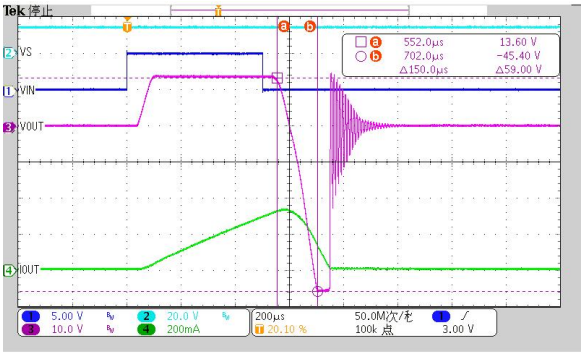
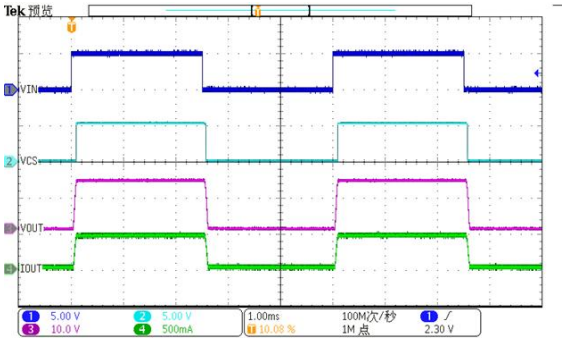


Figure 17. Inductive load switching-off waveform



V_{VS} = 13.5 V, current limit = 1 A, I_{OUTX} = 0.5 A, V_{INx} = 5 V at 200 Hz

Figure 18. PWM signal driving

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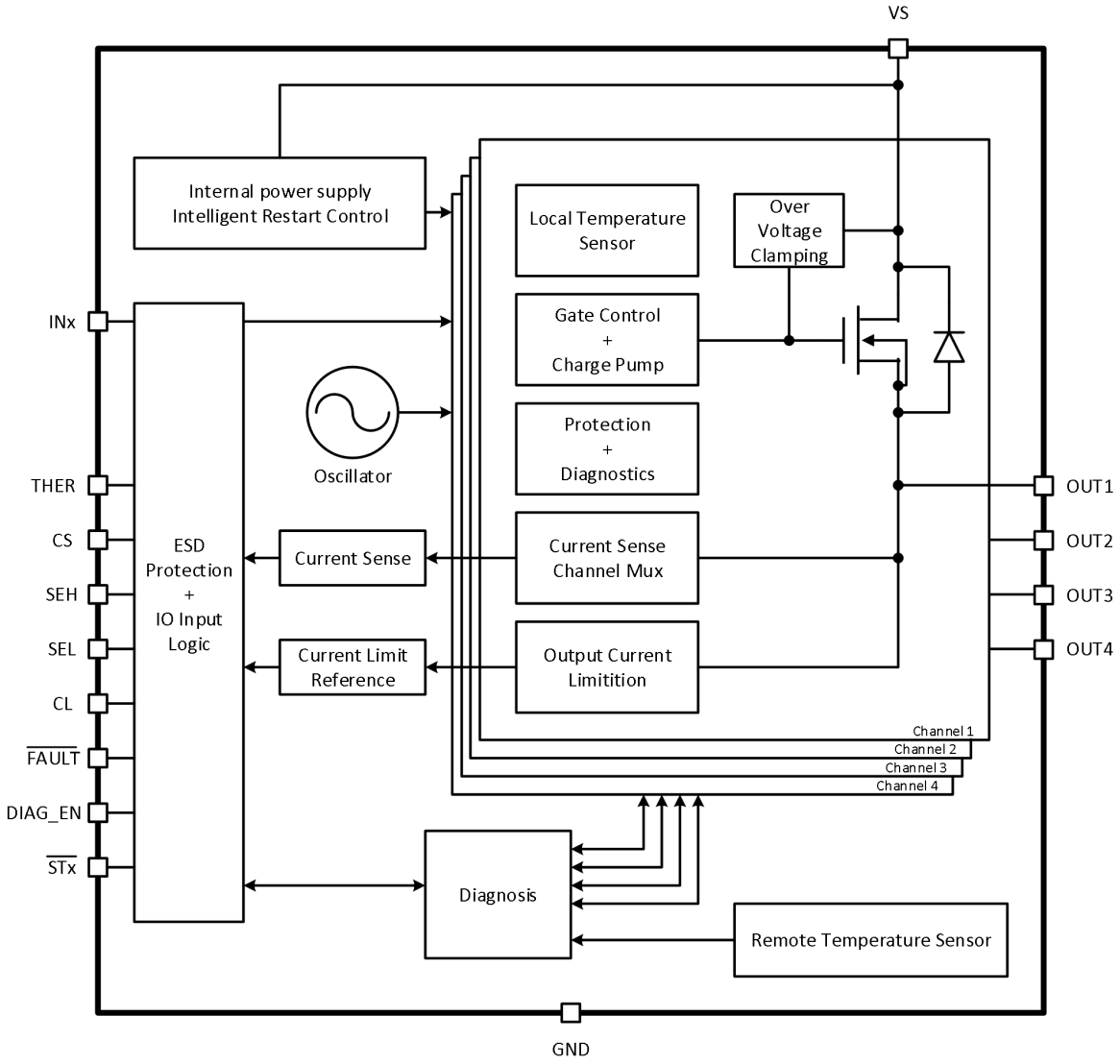
8. Block Diagram



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9. Function Description

9.1. Current sense

The high-accuracy current-sense function is available in the DIO74H120B, which improves real-time monitoring and enables a more accurate diagnostics without further calibration. The integrated current mirror is used to source 1 / $K_{(CS)}$ of the normal output load current. The maximum output voltage on CS pin is clamped to $V_{CS(H)}$, which is the fault voltage level.

The sense resistor value R_{CS} can be chosen to maximize the range of currents needed to be measured by the system, The R_{CS} value should be chosen based on application need.

— The maximum usable R_{CS} is bounded by the minimum voltage accepted by the external system, for the smallest load current needed to be measured by the system.

— The minimum acceptable R_{CS} value has to ensure the V_{CS} is below the $V_{CS(H)}$ value so that the system can detect faults.

— The maximum current the system wants to read needs to be below the current limit threshold, because once the current limit threshold is tripped, the V_{CS} will transmit to $V_{CS(H)}$.

As there's a fault occuring, the CS pin also works as a fault report with a pullup voltage, $V_{CS(H)}$. Please find more details below:

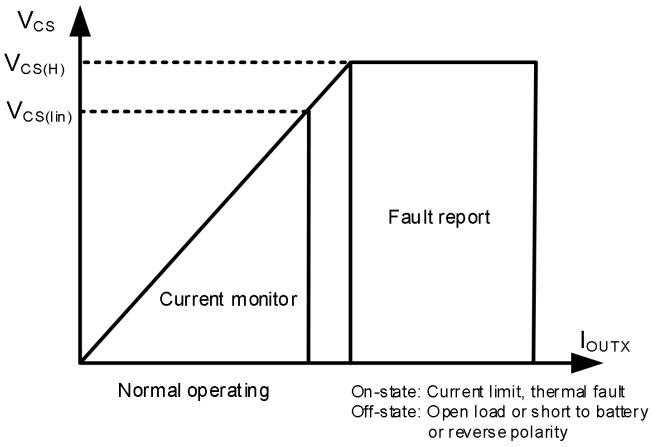

Figure 19. Current-sense output-voltage curve

9.2. Adjustable current limit

A high-accuracy current limit helps the device achieve higher reliability, which protects the power supply during short circuit or power up. If the thermal shutdown occurs, the current limit is set to $I_{CL(TSD)}$) to reduce the power dissipation on the power FET.

There are two current-limit thresholds.

— Internal current limit. The internal current limit is fixed at $I_{CL(int)}$. For large-transient-current applications, the CL pin is directly tied to the device GND.

— External adjustable current limit. An external resistor is used to set the current-limit threshold. $R_{(CL)}$ can

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be calculated with the equation (1):

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} \quad (1)$$

When using a GND network that results in a level shift between the device GND and board GND, it's a must to connect the CL pin with device GND.

In case of a hard short-to-GND condition, the DIO74H120 provides a fast-trip protection to turn off the related channel before the current-limit closed loop is set up.

9.3. Inductive-load switching-off clamp

When an inductive load is switched off, the output voltage is pulled down to negative due to the inductance characteristics. Battery energy and load energy are dissipated on the high-side power switch, which leads to the large thermal variation, The power FET may break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, $V_{DS(clamp)}$. For PWM-controlled inductive loads, it is recommended to add the external freewheeling circuitry to protect the device from repetitive power stressing.

Figure 17 shows a waveform if the device driving an inductive load. On the waveform, the duration of V_{OUT} from V_{VS} to (V_{VS} - $V_{DS(damp)}$) is approximately 150 µs. When the clamp is active, the switching-off slew rate is also optimized, which helps to minimize the effects of transient power and EMI. It's also shown that the controlled slew is approximately 0.4 V/µs.

For PWM-controlled inductive loads, DIOO reommends that a external freewheeling circuity should be added to protect the DIO74H120 from repetitive power stressing. TVS is used to achieve the fast decay.

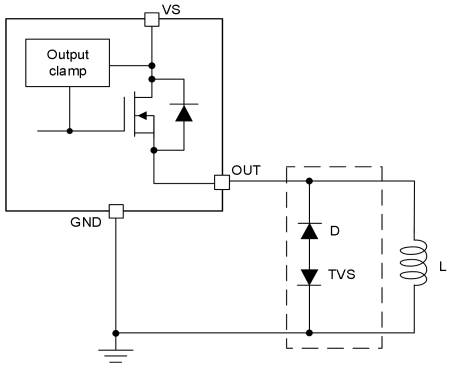

Figure 20 . Protection with external circuitry

9.4. Fault detection and reporting

9.4.1. Diagnosis configuration table

The DIAG_EN pin enables or disables the diagnostic functions.

For DIO74H120B, both SEL pin and SEH pin multiplex the shared current-sense function among the four channels.

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Table 1. Diagnosis configuration

DIAG_EN	INx	SEH	SEL	CS Activated Channel	CS, $\overline{FAULT}$, $\overline{STx}$	Protections & Diagnostics
L	H	-	-	-	High impedance	Diagnostics disabled, full protection
	L					Diagnostics disabled, no protection
H	-	0	0	Channel 1	(See table 2)	(See table 2)
		0	1	Channel 2		
		1	0	Channel 3		
		1	1	Channel 4		

9.4.2. Fault table

For DIO74H120A, four individual $\overline{STx}$ pins report the fault conditions, each pin for its respective channel; For DIO74H120B, a global $\overline{FAULT}$ pin is used to monitor the global fault condition among all the channels When a fault condition occurs, it pulls $\overline{STx}$ down to GND. A 3.3 or 5 V external pullup is required to match the supply level of the microcontroller.

The CS pin also works as a fault report with an internal pull-up voltage $V_{CS(H)}$.

Table 2. Fault table

Conditions	INx	OUTx	THER	Criterion	$\overline{STx}$ (1)	CS (2)	$\overline{FAULT}$ (2)	Fault Recovery
Normal	L	L	-	-	H	0	H	-
	H	H	-	-	H	In linear region	H	-
Overload, short to GND	H	L	-	Current limit triggered	L	$V_{CS(H)}$	L	Auto
Open load (3), short to battery, reverse polarity	L	H	-	V_{VS} - V_{OUTx} < $V_{(ol,off)}$	L	$V_{CS(H)}$	L	Auto
Thermal shutdown	H	-	L	T_{SD} triggered	L	$V_{CS(H)}$	L	Output auto-retry. Fault recovers when T_J < $T_{SD,rst}$ or when INx toggles.
			H					Output latch off. Fault recovers when INx toggles.
Thermal swing	H	-	-	T_{SW} triggered	L	$V_{CS(H)}$	L	Auto

Note:

(1) For DIO74H120A.

(2) For DIO74H120B.

(3) An external pullup is required for open-load detection.

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9.5. Full diagnostics

9.5.1. Short-circuit and overload protection

When a channel is on, the overcurrent appears in a short to GND or overload condition. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The device heats up if no actions are taken. If there's a thermal shutdown, the current limit, $I_{CL(TSD)}$, keeps the power stressing on the power FET to a minimum. When the fault condition is removed, the device automatically recovers.

9.5.2. Open-load detection

When a channel on, the open-load event can be detected as an ultra-low V_{CS} on CS pin. Note that the detection is not reported on the $\overline{STx}$ or $\overline{FAULT}$ pins. The microcontroller must multiplex the SEL and SEH pins to detect the channel-on open-load fault proactively.

When a channel off, if an open load occurs, the output voltage is close to the supply voltage($V_{VS} – V_{OUTx} < V_{(ol,off)}$), and the fault is reported out. There is always a leakage current $I_{(ol,off)}$ present on the output. The recommended pullup resistance is 20 kΩ to offset the leakage current.

9.5.3. Short-to-battery detection

Short-to-battery has the same detection mechanism and behavior as open-load detection.

In the on-state, reverse current flows through the FET rather than the body diode, which causes less power dissipation. Therefore, the worst case occurs in the off-state.

— If $V_{OUTx} – V_{VS} < V_{(F)}$ (body diode forward voltage), no reverse current occurs.

— If $V_{OUTx} – V_{VS} > V_{(F)}$, reverse current occurs. The current must be limited to less than $I_{R(1)}$.

9.5.4. Reverse polarity detection

Reverse polarity detection also has the same detection mechanism and behavior as open-load detection.

In the on-state, the reverse current flows through the FET rather than the body diode, which causes less power dissipation. Therefore, the worst case occurs in the off-state. The reverse current must be limited to less than $I_{R(2)}$.

9.5.5. Thermal fault detection

In case of the severe power stressing cases, the device has two types of thermal fault detection to protect the device: absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing).

Thermal shutdown is active when the absolute temperature $T_J > T_{SD}$. When thermal shutdown occurs, the respective output turns off. The THER pin is used to configure the behavior after the thermal shutdown occurs. When the THER pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the THER pin goes from high to low, thermal shutdown changes to auto-retry mode. The thermal shutdown fault signal is cleared after toggling the related INx pin.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} – T_{(Logic)} > T_{SW}$, then the output turns off. The output automatically recovers and the fault signal clears when

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$\Delta T = T_{(FET)} - T_{(Logic)} < T_{SW} - T_{HYS}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation.

9.6. Full protection

9.6.1. Undervoltage lockout (UVLO)

When V_{VS} falls down to $V_{VS(uvf)}$, the device shuts down. When V_{VS} rises up to $V_{VS(uvr)}$, the device turns on.

9.6.2. Loss-of-GND protection

When loss of GND occurs, output is shut down regardless of whether the INx pin is high or low. The device can protect against loss of device GND and loss of module GND condition.

9.6.3. Protection for loss of power supply

When loss of supply occurs, whether the input is high or low, the output is turned off.

For a resistive or capacitive load, loss of supply protection is easy to achieve due to no more power. But for a charged inductive load, the current is driven from all the I/O pins to maintain the inductance current. To protect the system in this condition, two types of external protections are recommended: the GND network or the external free-wheeling diode.

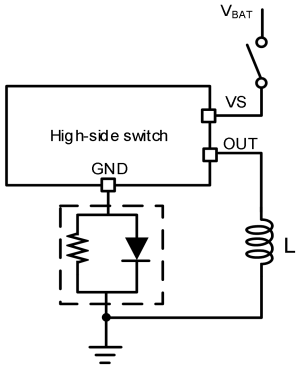

Figure 21. Protection for loss of power supply (type 1)

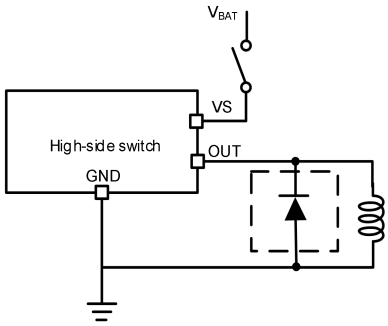

Figure 22. Protection for loss of power supply (type 2)

9.6.4. Reverse-current protection

There are two conditions where the reverse current occurs: short to battery and reverse polarity.

In a short-to-battery condition, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of

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the reverse current.

In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current.

To protect the device, two types of external circuitry are recommended: adding a blocking diode and the GND network.

For type 1, an anti-reverse diode is added between the supply and VS pin. Both the IC and load are protected when it's in reverse polarity.

For type 2, the reverse current through the device GND is blocked while the reverse current through the FET is limited by the load itself. A resistor is recommended to be in parallel with the diode as a GND network. For an diode more than 100 mA, a 1-kΩ resistor is recommended to select. The diode and resistor can be shared among devices if there are multiple high-side switches. The reverse current protection diode in the GND network forward voltage should be no more than 0.6 V. On I/O pins, the resistance is recommended to be 4.7 kΩ (min). Please be noted that there will be a large power dissipation on the GND network resistor when reverse polarity of the power supply occurs, the 1206 package for resistor is recommended.

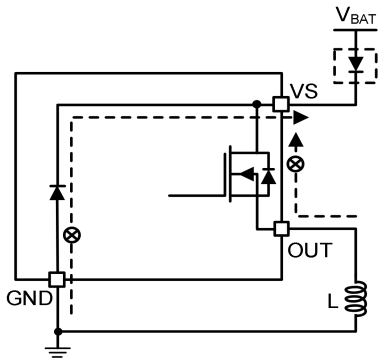

Figure 23. Reverse-current external protection (type 1)

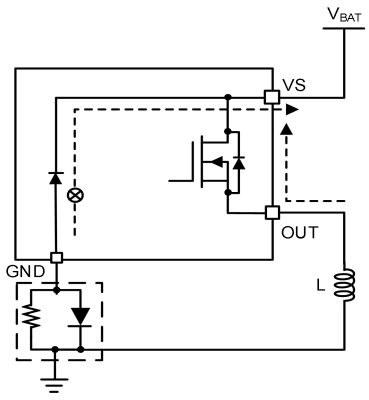

Figure 24. Reverse-current external protection (type 2)

9.6.5. MCU I/O protection

In some severe conditions, such as the loss of battery with inductive loads, a negative pulse occurs on the GND pin can cause damage on the connected microcontroller. It's recommended to use serial resistors to protect the microcontroller. For example, 10 kΩ is recommended for 5 V microcontroller.

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9.7. Device function modes

The DIO74H120 has three working modes: the normal mode, the standby mode and the the standby mode with diagnostics.

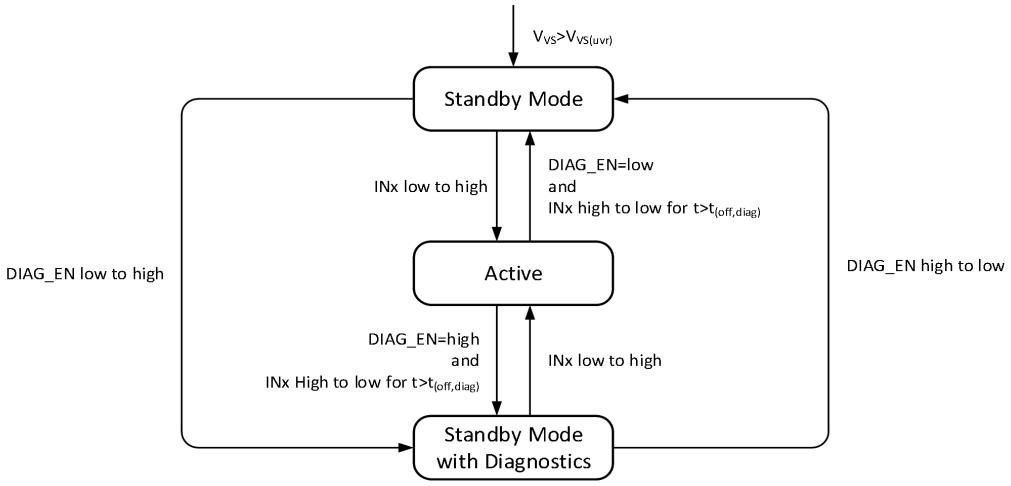

Figure 25. Working modes

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10. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

The DIO74H120 can drive various resistive, inductive and capacitive loads, including low-wattage bulbs, LEDs, relays, solenoids, heaters and sub-modules. Full diagnosis and high-precision current-sense can realize intelligent control of load. The external adjustable current limit can improve the reliability of the whole system by clamping surge or overload current.

10.1. Typical application

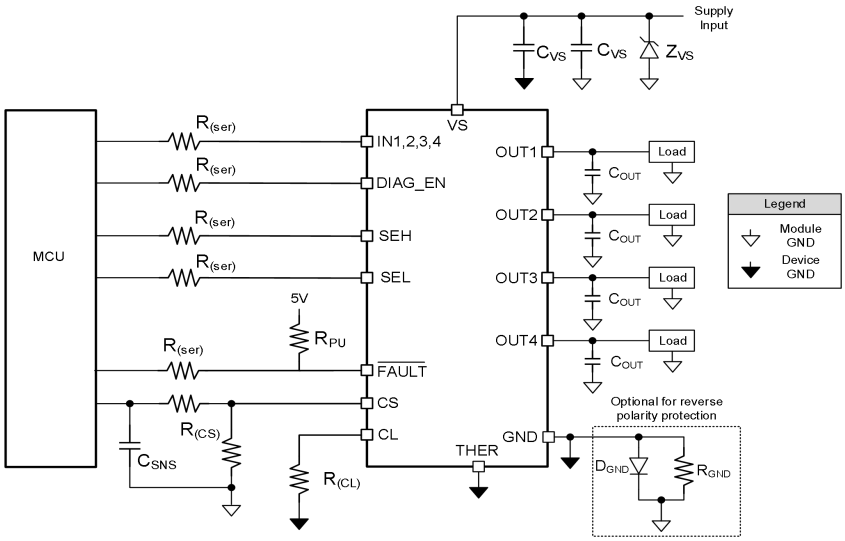

Figure 26. Typical applicaiton

With the ground protection network, the device ground will be offset relative to the microcontroller ground.

Table 3. Recommended external components

Component	Typical Value	Purpose
$R_{(ser)}$	10 kΩ	Protect microcontroller and device I/O pins
$R_{(CS)}$	1 kΩ	Translate the sense current into sense voltage
C_{SNS}	100 pF to 10 nF	Low-pass filter for the ADC input
R_{GND}	1 kΩ	Stabilize GND potential during turn-off of inductive load
D_{GND}	BAS21 diode	Protect device during reverse supply condition
$R_{(CL)}$	1 kΩ (typ)	Set current limiting value, short to IC GND to set the current limit to the internal setting
C_{VS}	10 nF to Device GND and 10 µF + 100 nF to module GND	Filtering of voltage transients (e.g. surge)
Z_{VS}	TVS to module GND	Clamp voltage spikes at the input
C_{OUT}	22 nF	Filtering of voltage transients (e.g. ESD)

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10.2. Detailed design

To maintain the 1-A nominal current within the current-sense range of 0 to 4 V, $R_{(CS)}$ can be calculated from the equation below. A 1% tolerance or better resistor is recommended for a more accurate current-sensing.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUT}} = \frac{4 \times 300}{1} = 1200\ \Omega \quad (2)$$

To set the adjustable current limit at 2 A, calculate $R_{(CL)}$ with equation below:

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{2000}{2} = 1000\ \Omega \quad (3)$$

For 5 V MCU, it's recommended to use 10 kΩ for I/O protection and a 10-kΩ pull up resistor.

10.3. Application curves

To find a test example of soft-start when driving a big capacitive load, please refer to Figure 15. To find an expanded waveform of the output current, please refer to Figure 16.

For the detail of a test example of PWM-mode driving, please refer to Figure 18.

11. Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. Though the EP-TSSOP and QFN package has great thermal impedance, it's still crucial for the design of the PCB layout. Good PCB design optimizes heat transfer, which is critical to the long-term reliability of the device.

The copper on the PCB enables the heat flow from package to the ambient. Thus, it's important to maximizing the copper efficiency when there's no heat sink attached to the the PCB on the other side of the package.

To optimize the thermal conductivity of the board, add as many thermal vias as possible directly below the thermal pad. All thermal vias should be plated shut or capped on the both sides of the board, preventing in solder voids. The solder coverage should be no less than 85% to ensure the reliability and performance.

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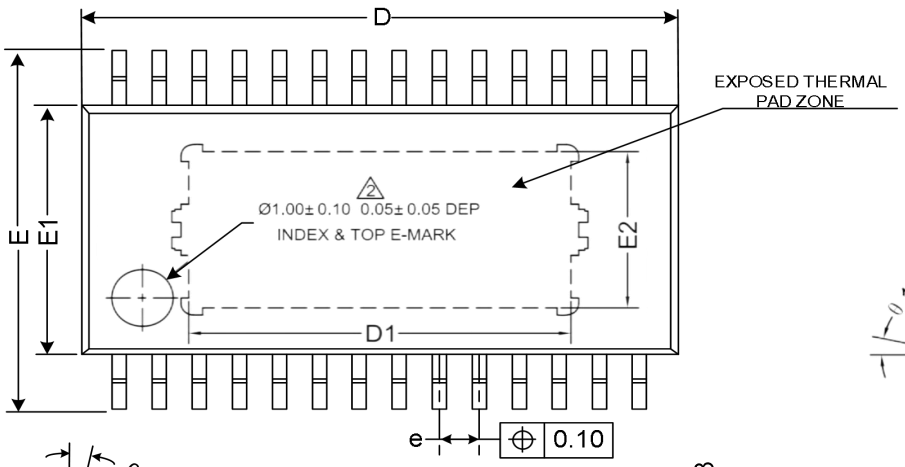
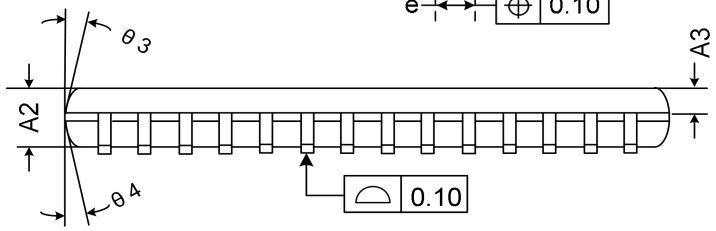
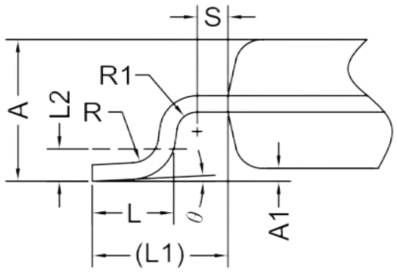
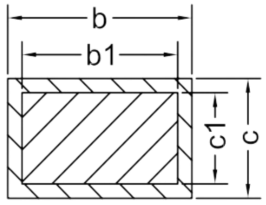
12. Physical Dimensions

12.1. EP-TSSOP28

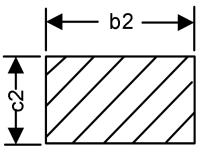








SECTION C-C
NORMAL PLATING



SECTION C-C
NIPdAu PLATING

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.10
A3	0.34	0.44	0.54
b	0.20	-	0.29
b1	0.19	0.22	0.25
b2	0.19	-	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
c1	0.12	-	0.14
D	9.60	9.70	9.80
D1		6.20 REF	
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2		2.75 REF	
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25 BSC	
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ	0°	-	8°
θ1	10°	12°	14°
θ2	10°	12°	14°
θ3	10°	12°	14°
θ4	10°	12°	14°

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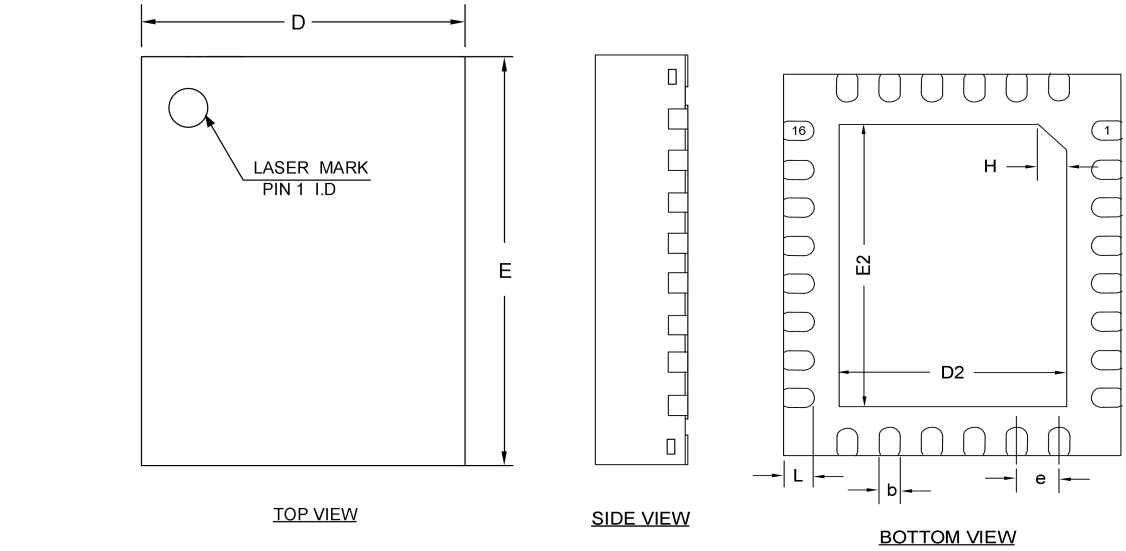
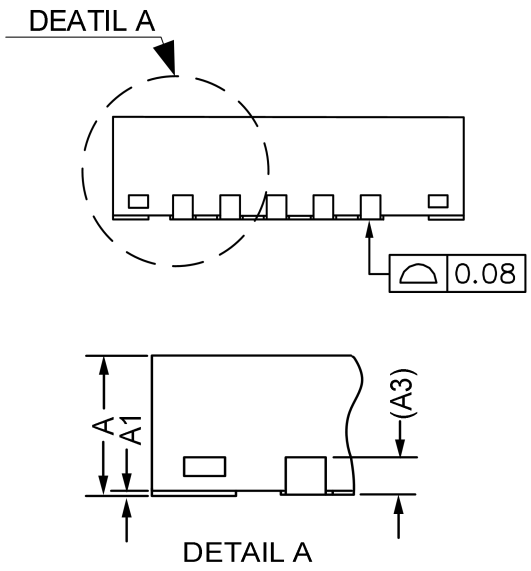
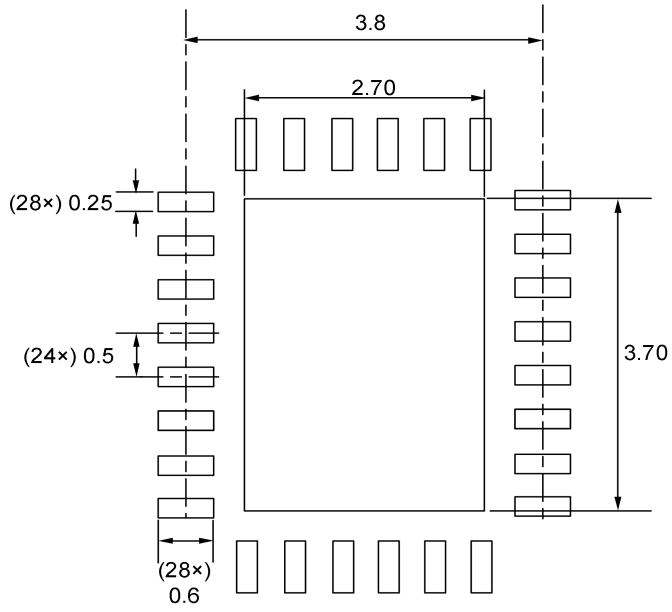
12.2. QFN4×5-28





Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	4.90	5.00	5.10
D2	2.65	2.70	2.75
E2	3.65	3.70	3.75
H		0.35 REF	
e	0.40	0.50	0.60
L	0.30	0.35	0.40



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