



# HK32APIN02x Datasheet

Version: 1.0

Release Date: 2022-10-31

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# Preface

## Purpose

This document introduces the block diagram, the memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32APIN02x Series SOC, to help users quickly understand its features and functions.

## Audience

This document is intended for:

- HK32APIN02x Developer
- HK32APIN02x Tester
- HK32APIN02x user

## Release Notes

This document is corresponding to HK32APIN02x Series SOC.

## Revision History

Version	Date	Description
0.1	2022/05/30	Alpha version release
1.0	2022/12/08	Official website version release

# Contents

1 Introduction .....	1
2 HK32APIN02x Overview .....	2
2.1 Features .....	2
2.2 Device overview .....	5
3 Function Description .....	8
3.1 Block diagram .....	8
3.2 Memory mapping.....	9
3.3 Memory .....	9
3.3.1 Flash.....	9
3.3.2 SRAM .....	9
3.4 CRC .....	9
3.5 Power Supply schemes .....	9
3.6 Power monitors .....	10
3.7 Boot mode .....	10
3.8 Low-power modes.....	10
3.9 Reset.....	10
3.9.1 System reset .....	10
3.9.2 Power reset .....	11
3.10 Clock and clock tree .....	12
3.11 NVIC .....	12
3.12 EXTI.....	14
3.13 GPIO .....	14
3.14 SYSCFG .....	14
3.15 DMA .....	15
3.16 COMP .....	15
3.17 OPAMP .....	15
3.18 DVSQ .....	15
3.19 EMACC .....	15
3.20 Timer .....	16
3.20.1 Advanced Timer .....	16
3.20.2 General-purpose Timer .....	16

3.20.3 SysTick Timer .....	17
3.21 ITRIM.....	17
3.22 Independent Watchdog.....	17
3.23 Window Watchdog.....	17
3.24 ADC.....	17
3.24.1 Temperature sensor .....	18
3.24.2 Internal reference voltage.....	18
3.25 I2C bus .....	18
3.26 USART.....	18
3.27 SPI.....	19
3.28 CAN .....	19
3.29 96-bit UID.....	19
3.30 Debug Interface .....	19
4 Electrical characteristics .....	20
4.1 Absolute maximum values.....	20
4.1.1 Voltage characteristics .....	20
4.1.2 Current characteristics .....	20
4.1.3 Thermal characteristics .....	20
4.2 Operation conditions .....	21
4.2.1 General operation conditions .....	21
4.2.2 PVD characteristics .....	22
4.2.3 BOR characteristics.....	22
4.2.4 POR/PDR characteristics .....	23
4.2.5 VREFINT characteristics.....	24
4.2.6 Operating current .....	24
4.2.7 HSE clock characteristics .....	24
4.2.8 LSE clock characteristics .....	25
4.2.9 High-speed internal (HSI) RC oscillator .....	26
4.2.10 Low-speed internal (LSI) RC oscillator .....	26
4.2.11 PLL characteristics .....	26
4.2.12 Flash memory characteristics .....	27
4.2.13 I/O port input characteristics.....	27

4.2.14 I/O port output characteristics .....	27
4.2.15 NRST reset pin characteristics .....	28
4.2.16 TIM timer characteristics .....	28
4.2.17 EMACC characteristics.....	28
4.2.18 ADC characteristics .....	28
4.2.19 Temperature sensor characteristics .....	32
4.2.20 DAC voltage divider characteristics .....	32
4.2.21 COMP characteristics .....	32
4.2.22 OPAMP characteristics .....	33
5 Power supply scheme.....	34
6 Pinouts and pin descriptions.....	34
6.1 LQFP48 .....	35
6.2 LQFP44 .....	36
6.3 LQFP32 .....	37
6.4 TSSOP24 .....	37
6.5 Pin description.....	38
6.6 AF function and pin mapping .....	47
7 Package characteristics.....	50
7.1 LQFP48 .....	50
7.2 LQFP44 .....	51
7.3 LQFP32 .....	52
7.4 TSSOP24 .....	53
8 Ordering information .....	56
9 Glossary and Abbreviations .....	57
10 Legal and Contact Information .....	58

# 1 Introduction

This document is the datasheet for HK32APIN02x series System-on-Chips (SOCs). HK32APIN02x is a family of economic motor-dedicated microcontrollers (MCU) developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd, including:

- HK32ASPIN020
  - HK32ASPIN020E8P7(TSSOP24)
  - HK32ASPIN020K8T7(LQFP32)
  - HK32ASPIN020S8T7(LQFP44)
- HK32ASPIN021
  - HK32ASPIN021K8T7(LQFP32)
  - HK32ASPIN021C8T7(LQFP48)
- HK32ASPIN022
  - HK32ASPIN022K8T7(LQFP32)
  - HK32ASPIN022C8T7(LQFP48)

## 2 HK32APIN02x Overview

HK32APIN02x is a motor-dedicated microcontroller, which integrates Hangshun self-dependent researched EMACC (Electrical motor accelerator) module. It incorporates the high-performance ARM® Cortex™-M0 32-bit RISC core operating at up to 80 MHz frequency, carrying high-speed embedded memories (up to 60 Kbytes of Flash memory and 8 Kbytes of SRAM).

HK32APIN02x is embedded with one 16-bit advanced timer, of which, four channels support PWM output, three of the four channels have asymmetric dead-time complementary PMW output; one 32-bit general-purpose timer, and four 16-bit general-purpose timers.

The internal analog circuitry of HK32APIN02x includes: one 12-bit ADC (two simultaneous sample/host channels, 16 channels), two analog operation amplifiers (PDA mode), three analog voltage comparators (PGA thresholds), one POR/PDR, one temperature sensor and one internal reference voltage.

Excepts the power supply, ground and NRST pins, all rest pins of HK32APIN02x are able to worked as GPIO, peripheral IO or EXTI input IO; in the pin-restricted scenarios, HK32APIN02x provides as much pins as possible, and all IOs support 5V tolerant input/output.

HK32APIN02x supports traditional Flash read/write protection, and also supports Hangshun self-dependent researched Flash code encryption. Meanwhile, to support various security applications, it provides CRC parity function, for the data integrity verification and data encryption/decryption. By configuring the Flash control register, it implements the remapping of interrupt vector to Flash domain.

HK32APIN02x offers standard communication interfaces: one I2C, one SPI, six UARTs and one bxCAN.

HK32APIN02x integrates Division and square root (DVSQ) module, which enhances ability of software processing and external event responding.

HK32APIN02x supports Sleep and Stop low-power consumption modes, allows the design of low-power applications.

These features make the HK32APIN02x microcontrollers suitable for a wide range of applications of BLDC/PMSM motors, or FOC driving control:

- Electrical tools
- Industrial fans
- Compressors
- Electrical vehicle
- Kitchen ventilator
- Vacuum sweeper
- Water pump
- Ceiling fan
- Air conditioner

### 2.1 Features

- CPU core
  - ARM® Cortex®-M0 core
  - Maximum frequency: 80 MHz
  - 24-bit SysTick timer
  - Interrupt vector remapping supported (via the configuration of Flash registers)
- Operating voltage range

- Single power supply ( $V_{DD}$ ): 2.2 V to 5.5 V
- Operating temperature range:  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$
- Typical operating current
  - Run mode: 1.8 mA@3.3V
  - Sleep Mode: 364  $\mu\text{A}$ @3.3V
  - Stop mode: 361 $\mu\text{A}$ @3.3V
- Memory
  - 60 Kbytes Flash
    - When the CPU frequency is not more than 24 MHz, MCU supports zero wait state.
    - Flash data security protection function (read or write protection can be set respectively)
    - Instructions and data stored in Flash can be encrypted to protect from physical attack.
  - 8Kbyte SRAM
- Clock
  - External high-speed clock (HSE): 4-24 MHz (typical value: 8 MHz)
  - External low-speed clock (LSE): 32.768 kHz
  - Internal high-speed clock (HSI): 8 MHz/14 MHz/56 MHz
  - Internal low-speed clock (LSI): 32.768 kHz
  - PLL clock: 1~80MHz
  - External input clock: 5~30MHz
- Reset
  - External pin reset
  - Option byte loader reset
  - Watchdog timer reset (IWDG and WWDG)
  - Power reset (POR/PDR/BOR)
  - Software reset
- Programmable voltage detection (PVD)
  - 14 programmable thresholds
  - Programmable detecting condition (rising or falling edge)
- GPIO
  - Up to 42 GPIOs
  - Each GPIO supports 5V signal input/output
- DMA controller
  - 2 DMAs (DMA1/DMA2), each with 5 channels
  - Supports several peripherals triggering, such as Timer, ADC, SPI, I2C, USART.
- Data communication interfaces
  - 6 x UARTs
  - 1x I2C
    - 1MHz/400kHz/100kHz transmission rate
    - In Stop mode, I2C supports the waking up function upon data reception
  - 1 x high-speed SPI (max 18Mbps transmission rate)
  - 1 x 2.0A/2.0B CAN

- Timer
  - 1 x advanced motor dedicated timer: TIM1
    - 4 PWM output channels, in which 3 with asymmetric dead-time complementary PMW output
    - Supports external pin signal break, and internal comparator output signal break
    - Supports CC1~CC6 multiple point comparison output triggering ADC
  - 5 x general-purpose PWM timers:
    - 32-bit: TIM2
    - 16-bit: TIM3/TIM14/TIM15/TIM16
- DVSQ
  - Supports 32-bit fix-point dividing operation, with simultaneous quotient and remainder obtained.
  - Supports 32-bit fix-point squaring root operation, with high resolution
- EMACC (Electrical motor accelerating hardware unit)
  - Supports Cordic operation, for sine-cosine operation
  - Supports Clarke, Park and reverse-Park operation
  - Supports SVPWM
  - Supports 1-channel high-speed motor data transmission (Trace)
- On-chip analog circuitry
  - 1 x12-bit 2-channel sampling-holding SAR ADC (up to 16 channels for analog signal input)
    - Maximum conversion rate: 2 MSPS(12-bit)
    - 2 independent sampling-holding units, support simultaneous sampling for the same signal
    - Supports 4 independent queues and 1 test queue conversion
    - Supports automatic continuous conversion, and scanning conversion
    - Supports in-queue channel-replacing
    - Supports multiple hardware trigger resources (TIM1\_TRGO、TIM1\_CCx、GPIO input events)
    - Supports multiple sampled data to be averaged
    - Independent channel result register
  - Internal reference voltage
    - Internal reference voltage output connected to ADC independent channel
  - Temperature sensor
    - Temperature sensor is connected to ADC independent channel
  - 3 x voltage comparators
    - The reference voltage of the comparator can be the external signal input or from the internal 8-bit DAC
    - Comparator output can work as a break signal of an advanced timer
  - 2 x operation amplifiers
    - Programmable amplification factor
    - Amplifier export pin can be the sampling channel of ADC
- 96-bit unique ID
  - Works as the series number and security key
  - Activates the security self-boot process
- CPU trace and debug

- SWD debug interface
- ARM® CoreSight™ debug components (ROM-Table, DWT and BPU) debug components
  - Self-designed DBGMCU controller (low power mode simulation control, debug peripheral clock control, debug and trace interface allocation)

## 2.2 Device overview

Table 2-1 HK32APIN02x series features

Features	HK32ASP IN 021C8T7	HK32ASP IN 022C8T7	HK32ASP IN 020S8T7	HK32ASP IN 020K8T7	HK32ASP IN 021K8T7	HK32ASP IN 022K8T7	HK32ASP IN 020E8P7
GPIO	42	41	40	29	28	27	21
Package	LQFP48		LQFP44	LQFP32			TSSOP24
Operating voltage	2.2V~5.5V						
Operating temperature	-40°C ~ +105°C						
Memory	Flash	60 Kbyte					
	SRAM	8 Kbyte					
CPU	Core	Cortex®-M0					
	CPU frequency	80MHz					
DMA (Channels)	2 (each has 5 channels)						
DVSQ	1						
Clock	LSI	32.768kHz					
	HSI	configurable: 8MHz/14MHz/56MHz					
	PLLCLK	supported					
	HSE	4~24MHz					
	LSE	32.768kHz			not supported		
Timers	Advanced timer	1 x (16-bit): TIM1					
	General-purpose timer	1 x (32-bit): TIM2 4 x (16-bit): TIM3/TIM14/TIM15/TIM16					
	System Tick	1					
	IWDG	1					
	WWDG	1					
	Communication peripheral	UART	6				
I2C		1					
SPI		1					not supported
CAN		1					
ITRIM	1						

Features		HK32ASP IN 021C8T7	HK32ASP IN 022C8T7	HK32ASP IN 020S8T7	HK32ASP IN 020K8T7	HK32ASP IN 021K8T7	HK32ASP IN 022K8T7	HK32ASP IN 020E8P7
A D C	ADC (external analog channels)	1 (12)	1(12)	1(12)	1(10)	1(10)	1(10)	1(9)
	Reference selection	Internal reference voltage						
	ADC conversion rate	2 MSPS (12-bit)						
	ADC resolution	12-bit						
Temperature Sensor		1						
COMP		3						
OPAMP		2						
EMACC		1						
PVD		1						
CRC		1						
96-bit UID		1						

## 3 Function Description

### 3.1 Block diagram

HK32ASPIN02x integrates a 60 Kbytes Flash, for instruction and data storage.

It is embedded with ARM® Cortex®-M0, a 32-bit RISC processor, which provides an economic motor-dedicated MCU platform, and delivers outstanding computational performance and an advanced interrupt response system. HK32APIN02x family is compatible with ARM tools and software.

Taking the HK32ASPIN021C8T7 as an example, the block diagram of HK32APIN02x is as follows:

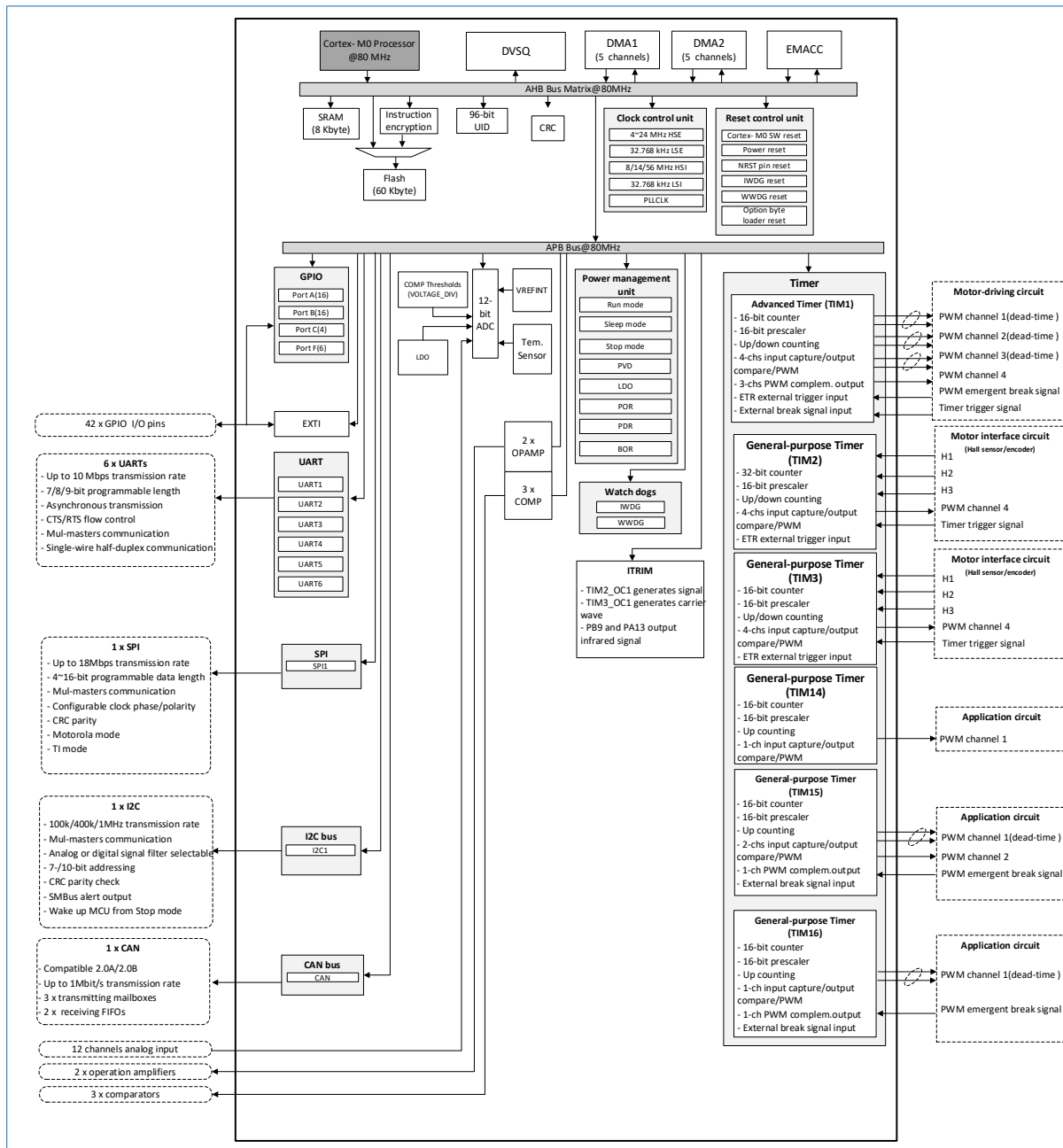


Figure 3-1 HK32ASPIN021C8T7 block diagram

## 3.2 Memory mapping

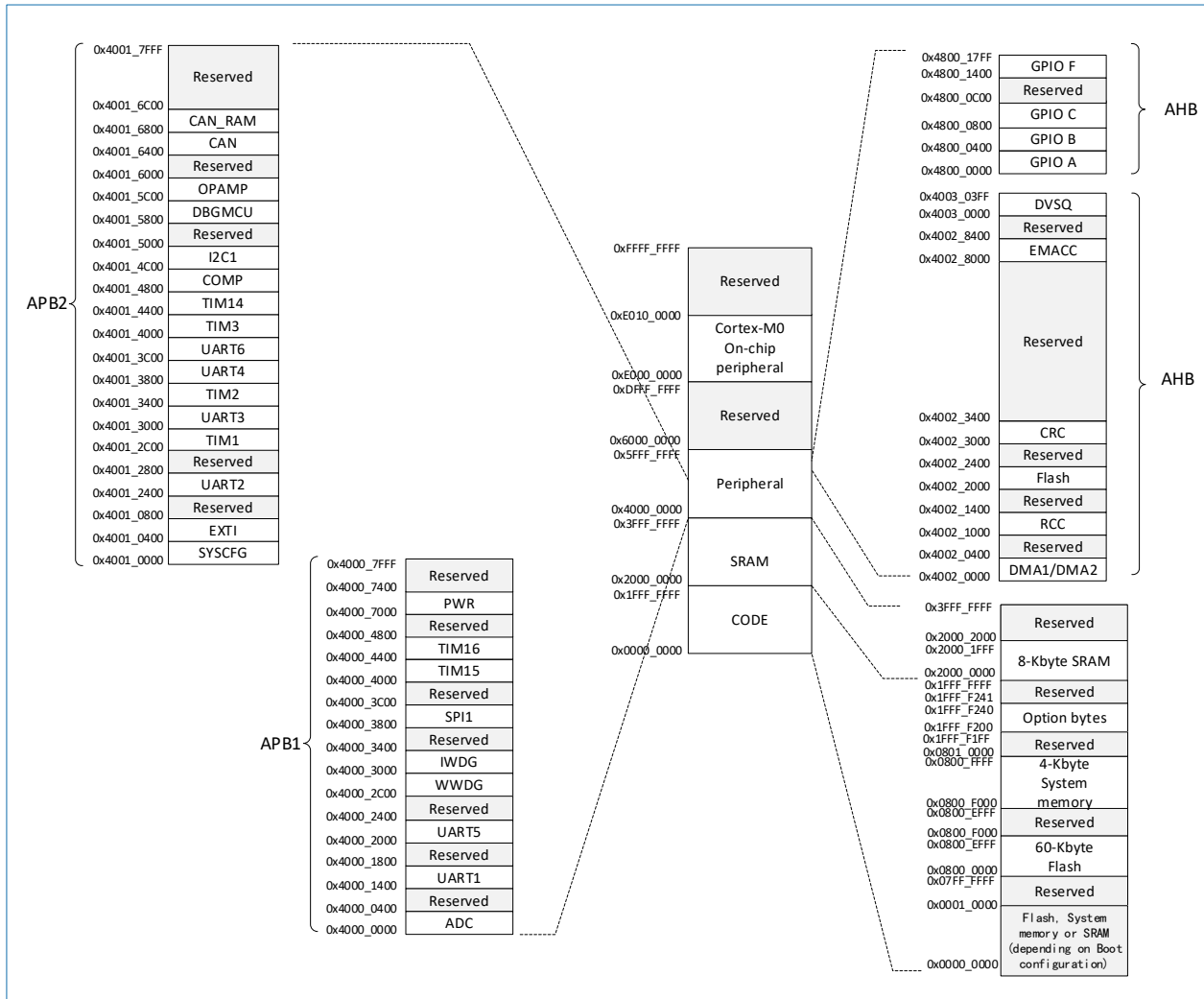


Figure 3-2 Memory mapping

## 3.3 Memory

### 3.3.1 Flash

HK32APIN02x integrates a Flash memory up to 60 Kbytes to store programs and data.

### 3.3.2 SRAM

HK32APIN02x integrates an 8 Kbyte SRAM, and supports word-, half-word-, and byte-, access. CPU can access SRAM fast with zero wait state to meet the requirements of most applications.

## 3.4 CRC

CRC is used to verify data transmission or storage integrity. HK32APIN02x integrates a CRC calculation unit to reduce user application processing burden and to provide the ability to accelerate processing.

CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 3.5 Power Supply schemes

- $V_{DD}$ : 2.2V~5.5V

The  $V_{DD}$  supplies power for on-chip digital circuitry, I/O pins and internal LDO.

## 3.6 Power monitors

HK32APIN02x embeds POR/PDR/BOR circuitry. The circuitry always operates to ensure the system runs well with a power supply above 2.2V. When  $V_{DD}/V_{DDA}$  is less than the POR/PDR threshold ( $V_{POR}/V_{PDR}$ ), MCU remains reset state without an external reset circuit needed. During the power-on process, BOR keeps MCU in reset state, till the voltage reaches the programmed BOR threshold (VBOR). When BOR is disabled, the power off reset is managed by the PDR circuit.

HK32APIN02x integrates a programmable voltage detector (PVD). The PVD monitors the  $V_{DD}$  power supply and compare it with the  $V_{PVD}$  threshold. When  $V_{DD}$  is below or over the  $V_{PVD}$  threshold, an interrupt is generated. The interrupt program sends an alarm warning or switches MCU into Safe mode. PVD starts after it is enabled.

## 3.7 Boot mode

The Boot pin is used to select one of the following modes when the system starts:

- Boot from Flash block
- Boot from the system memory
- Boot from the internal SRAM

Bootloader program is stored in the system memory and it can reprogram Flash via the USART1 or PA8/PA9 interfaces.

## 3.8 Low-power modes

HK32APIN02x supports two low-power modes:

- Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

In Stop mode, MCU achieves the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all internal clocks, the PLL, the HSE oscillators and the HSI oscillators are disabled. MCU can be woken up from Stop mode by any EXTI line. The EXTI line source can be any one of the external I/O pins.

I2C1 supports waking up MCU from stop mode by receiving data.

## 3.9 Reset

HK32APIN02x supports System reset and Power reset.

### 3.9.1 System reset

Except for the reset flags in the RCC\_CSR register and registers in the backup domains, System reset signal resets all the registers.

When any of the following events occurs, a System Reset signal is generated:

- Low-level voltage on NRST pin (External Reset)
- Window watchdog counting terminates (WWDG Reset)
- Independent watchdog counting terminates (IWDG Reset)
- Software reset (SW Reset)
- Power reset (POR/PDR/BOR)

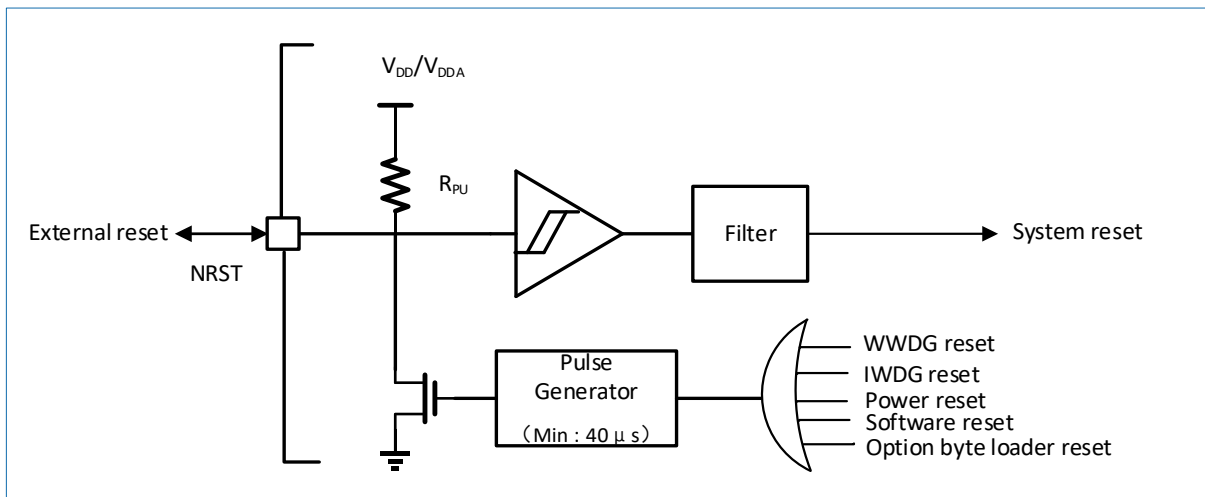


Figure 3-3 System reset

An Internal Reset signal is output via the NRST pin. A Pulse generator guarantees that each reset source produces at least 40  $\mu\text{s}$  pulse latency. When the NRST pin is pulled down and a reset pulse is generated for an external reset.

You can identify a reset source by checking reset state flags in the RCC\_CSR register.

### 3.9.2 Power reset

Power reset signal resets all registers except for the registers in the backup domain. The reset source affects the reset pin, and keeps a low level in the progress of reset. Reset entry vector is fixed on address 0x0000\_0004.

When the following event occurs, a Power reset signal is generated:

- POR/PDR reset
- BOR reset

HK32APIN02x embeds POR/PDR circuits. The circuits always operate to ensure the system runs well when power supply is over than POR/PDR threshold. When  $V_{DD}$  is less than the POR/PDR threshold, MCU resets and no external reset circuit is required.

HK32APIN02x embeds BOR circuits. BOR is disabled by default, the power is monitored by POR/PDR. The BOR can be enabled/disabled by programming the option byte.



- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Supports for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

Table 3-1 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0x0000 0000
-	-3	Fixed	Reset	Reset	0x0000 0004
-	-2	Fixed	NMI	Non-maskable interrupt	0x0000 0008
-	-1	Fixed	HardFault	All classes of fault	0x0000 000C
-	3	Settable	SVCall	System service call via SWI instruction	0x0000 002C
-	5	Settable	PendSV	Pendable request for system service	0x0000 0038
-	6	Settable	SysTick	System tick timer	0x0000 003C
0	7	Settable	WWDG	Window Watchdog interrupt	0x0000 0040
1	8	Settable	PVD	PVD interrupt (Combined with EXTI 16)	0x0000 0044
2	9	Settable	-	Reserved	0x0000 0048
3	10	Settable	FLASH	Flash global interrupt	0x0000 004C
4	11	Settable	RCC	RCC global interrupt	0x0000 0050
5	12	Settable	EXTI0_1	EXTI Line[1:0] interrupt	0x0000 0054
6	13	Settable	EXTI2_3	EXTI Line[3:2] interrupt	0x0000 0058
7	14	Settable	EXTI4_15	EXTI Line[15:4] interrupt	0x0000 005C
8	15	Settable	DMA1_CH1	DMA1 Channel 1 interrupt	0x0000 0060
9	16	Settable	DMA1_CH2_3	DMA1 Channel 2/3 interrupt	0x0000 0064
10	17	Settable	DMA1_CH4_5	DMA1 Channel 4/5 interrupt	0x0000 0068
11	18	Settable	ADC	ADC global interrupt	0x0000 006C
12	19	Settable	TIM1	TIM1 global interrupt	0x0000 0070
13	20	Settable	UART1	UART1 global interrupt	0x0000 0074
14	21	Settable	TIM2	TIM2 global interrupt	0x0000 0078
15	22	Settable	TIM3	TIM3 global interrupt	0x0000 007C
16	23	Settable	UART3	UART3 global interrupt	0x0000 0080
17	24	Settable	UART4	UART3/4 global interrupt	0x0000 0084
18	25	Settable	TIM14	TIM14 global interrupt	0x0000 0088
19	26	Settable	TIM15	TIM15 global interrupt	0x0000 008C
20	27	Settable	TIM16	TIM16 global interrupt	0x0000 0090
21	28	Settable	DMA2_CH1	DMA2 Channel 1 interrupt	0x0000 0094
22	29	Settable	DMA2_CH2_3	DMA2 Channel 2/3 interrupt	0x0000 0098
23	30	Settable	DMA2_CH4_5	DMA2 Channel 4/5 interrupt	0x0000 009C
24	31	Settable	I2C1_SPI1	I2C1 and SPI1 global interrupt (Combined with EXTI21)	0x0000 00A0
25	32	Settable	UART2	UART2 global interrupt	0x0000 00A4

Position	Priority	Name	Description	Address	
26	33	Settable	EMACC	EMACC global interrupt	0x0000 00A8
27	34	Settable	CAN	CAN global interrupt	0x0000 00AC
28	35	Settable	DVSQ	DVSQ global interrupt	0x0000 00B0
29	36	Settable	COMP1_COMP2_COMP3	COMP1/COMP2/COMP3 global interrupt (Combined with EXTI18/19/20)	0x0000 00B4
30	37	Settable	UART5	UART5 global interrupt	0x0000 00B8
31	38	Settable	UART6	UART6 global interrupt	0x0000 00BC

### 3.12 EXTI

The extended interrupts and events controller (EXTI) manages the external and internal asynchronous events/interrupts and generates the event request to the CPU/Interrupt Controller and a wake-up request to the Power Manager.

The active edge of each external interrupt line can be chosen independently, whilst for fixed interrupt the active edge is always the rising one. An interrupt could be left pending: in the case of a settable one, a status register is instantiated and indicates the source of the interrupt; an event is always a simple pulse and it's used for triggering the core Wake-up (e.g. Cortex-M0 RXEV pin). For fixed interrupts, the pending status is assured by the generating IP, so no need for a specific flag. Each input line can be masked independently for interrupt or event generation, in addition the fixed lines are sampled only in Stop mode. This controller allows also to emulate the (only) external events by software, multiplexed with the corresponding hardware event line, by writing to a dedicated register.

HK32APIN02x embeds 32 external interrupt/event controller (EXTI) lines.

- 20 settable EXTI line
  - Both rising and falling edges can be configured as triggering edge
  - Dedicated interrupt status flag
  - The trigger interrupt or event could be configured by software
- 1 fixed EXTI line
- Each EXTI line could be masked or triggered respectively
- Detect the external signal whose pulse width is narrower than the APB2 clock width

### 3.13 GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as a peripheral alternate functional. Most of the GPIO pins are shared with digital or analog alternate functional. All GPIOs are high current capable. The I/Os alternate function configuration can be locked to avoid spurious writing to the I/O registers.

### 3.14 SYSCFG

The devices feature a set of configuration registers. The main purposes of the system configuration controller are the following:

- Enabling/disabling I2C Fast Mode Plus on some IO ports.
- Remapping the UART CTS function as RX function, likewise, RTS function as TX function.
- Remapping the memory located at the beginning of the code area.
- Managing TIM3\_CH4 input remapping to LSI, HSI, and LSE signals.
- Managing the external interrupt line connection with the GPIOs.
- Configuring VOLTAGE\_DIV of 8-bit DAC.

### 3.15 DMA

HK32APIN02x embeds 2 DMAs (DMA1/DMA2), each has 5 channels. The two DMA manages transfers from memories to memories, devices to memories, and memories to devices.

DMA can be used with the main peripherals. Each DMA has one arbiter to manage the priority of different DMA requests.

- Each DMA has 5 independent configurable channels.
- Every channel has a dedicated hardware DMA request logic and can be triggered by software.
- The DMA supports circular buffer management.
- Supports remapping of DMA requests from TIM1/2/3/15/16, SPI1, UART1/2/3/4/6, I2C1 and ADC.

### 3.16 COMP

HK32APIN02x embeds 3 ultra-low power voltage comparators (COMP1/2/3). These 3 comparators can be separately used with respective GPIO interfaces, for motor controlling, or cooperate with timers.

- When triggered by an analog signal, the COMP can wake up the MCU from STOP mode.
- Working for analog signal regulation.

### 3.17 OPAMP

HK32APIN02x embeds 2 operation amplifiers (OPAMP1/2). They can be configured flexibly, and used for weak signal amplifying, and motor implementation. OPAMP1/2 can be configured inverted or non-inverted, with different gain combinations, and can be cascaded with external resistor(s).

### 3.18 DVSQ

Division and square root calculation (DVSQ) unit features:

- Supports 32-bit signed/unsigned number multiplication and 32-bit unsigned number square root operations.
  - DVSQ unit supports only one of division and square root operations at the same time.
  - After 32-bit signed/unsigned integer division operations completes, the quotient and the remainder of which are obtained simultaneously and updated in the corresponding register.
  - Unsigned number square root operations can be set by software to operate with high accuracy.
  - Division operations support MOD operations.
- Pipeline design: 2-bit calculation is completed in every clock period.
- Calculation time depends on numbers in the operation.
- Supports dividing by zero interrupts and overflow interrupts.

### 3.19 EMACC

EMACC (Electrical motor accelerator) is used for a brushless DC motor controlled by FOC (Field Oriented Control) algorithm. EMACC can accelerate arithmetical operation driven by a motor. The operation speed is faster than software operation, with less CPU occupation. Under the same CPU frequency, it can support higher motor revolving speed, and enhance the driven frequency.

The device supports hardware operation, such as Cordic operation, Clarke conversion, Park conversion, reverse-Park conversion, PID algorithm, and SVPWM module, which takes the CPU a long time to operate. User inputs parameter:  $I_a$ ,  $I_b$ ,  $\theta$ , the EMACC operates and outputs the SVPWM, with a duty ratio of  $CNTPHA \setminus B \setminus C$ . In this way, the FOC operation time is saved.

The device embeds a digital tracer (EMACC\_TRACE), which actually is a high-speed hardware serial interface

module. It is used to export the EMACC parameters during motor adjustment, or high-speed running time. It provides 4 bytes for user-defined data output, making the motor adjustment easier.

The operation efficiency is highly enhanced by EMACC.

### 3.20 Timer

HK32APIN02x integrates an advanced timer (TIM1), and 5 general-purpose timers (TIM2/TIM3/TIM14/TIM15/16).

Table 3-2 Timer features

Timer	Name	Counter resolution	Counter type	Prescaler factor	DMA request	Break input	Capture/compare channel	Complementary output
Advanced timer	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	Yes	4	3
General-purpose timer	TIM2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	No	4	No
	TIM3	16-bit	up, down, up/down	Any integer between 1 and 65536	Yes	No	4	No
	TIM14	16-bit	up	Any integer between 1 and 65536	No	No	1	No
	TIM15	16-bit	up	Any integer between 1 and 65536	Yes	Yes	2	1
	TIM16	16-bit	up	Any integer between 1 and 65536	Yes	Yes	1	1

#### 3.20.1 Advanced Timer

The advanced timers (TIM1) can be seen as a three-phase PWM on 6 channels, and used as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output comparison
- PWM generation (edge or center-aligned modes)
- One-pulse mode output
- Complementary PWM outputs with programmable inserted dead-times

If configured as a standard 16-bit timer, an advanced timer has the same functions as the general-purpose timer. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%). Because most of its internal structure is the same as that of a general-purpose timer, the advanced timer can work together with general-purpose timers via Timer Link feature for synchronization or event chaining. In debug mode, the counter can be frozen.

#### 3.20.2 General-purpose Timer

Every general-purpose timer can generate a PWM output and can be used as a time base.

- TIM2 and TIM3

TIM2/3 provides a 32-bit (TIM2) or 16-bit (TIM3) auto-reload up/down counter, a 16-bit prescaler, and 4

independent channels. Every channel can be used for input capture, output compare, PWM, and a single pulse output. Up to 12 input captures, output compares and PWMs are provided in the maximum package.

TIM3 can cooperate with advanced timers through the Timer Linking feature for synchronization and event chaining. TIM3 supports an independent DMA request mechanism. TIM3 is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors. In debug mode, the counter can be frozen.

- TIM14 and TIM15

TIM14 and TIM15 provide a 16-bit auto-reload up counter, and a 16-bit prescaler. TIM14 has a channel for input capture, output compare, PWM and single pulse output. In debug mode, the counter can be frozen. TIM14 can't generate a DMA request, but TIM15 can.

- TIM16

TIM16 provides a 16-bit auto-reload up counter, and a 16-bit prescaler. TIM16 has a channel for input capture, output compare, PWM, and single pulse output. TIM16 has complementary PWM outputs with programmable inserted dead-times and can generate DMA requests.

### 3.20.3 SysTick Timer

SysTick timer is dedicated to the operating system as a standard down counter. It features:

- 24-bit down counter
- Auto-reload capability
- Generate a maskable interrupt when the counter reaches 0.
- Programmable clock source

### 3.21 ITRIM

HK32APIN02x integrates an infrared interface (IRTIM) for remote control. It can be used with an infrared LED to perform remote control functions.

To generate the infrared remote controlling signals, the IR interface (PB9/PA13) must be enabled and TIM2 channel 1 (TIM2\_OC1) and TIM3 channel 1 (TIM3\_OC1) must be properly configured to generate correct waveforms.

The infrared receiver can be implemented easily through a basic input capture mode of any timer.

### 3.22 Independent Watchdog

Independent watchdog (IWDG) is clocked from an internal independent 40 kHz RC. The IWDG is based on a 12-bit down counter and an 8-bit prescaler. Because it is independent from the main clock, IWDG can operate in Stop mode and Standby mode. It can be used as a watchdog to reset the system when a problem occurs or as a free running timer for application timeout management. IWDG can be configured to a software or hardware watchdog through Option bytes. In debug mode, the counter can be frozen.

### 3.23 Window Watchdog

Window watchdog (WWDG) is based on a 7-bit down counter. The counter can be set to the free running mode or used as a watchdog to reset the system when a problem occurs. It is clocked from the main clock and has an early warning interrupt capability. In debug mode, the counter can be frozen.

### 3.24 ADC

HK32APIN02x embeds a 12-bit ADC. The ADC has up to 12 external channels, and 4 internal channels. The analog-digital conversion of different channels can be performed in single, continuous, scan, or discontinuous modes.

ADC main features:

- When the maximum clock frequency of 28 MHz is reached, the ADC conversion rate can achieve 2MSPS.
- The ADC can be served by DMA.
- Flexible queue configuration: 4 independent conversion queues, and 1 test queue.
- Flexible arbitration mechanism, 0-3 priority level of each queue, larger number means higher priority.
- Independent result register for each channel, to restore the current conversion result.
- Trigger latency configuration allows latency of ADC conversion after the trigger signal generation.
- The event generated by the TIM1/2/3/15 is able to connect to ADC, to trigger A/D conversion.

### 3.24.1 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. It is used to measure the ambient temperature.

### 3.24.2 Internal reference voltage

Internal reference voltage ( $V_{REFINT}$ ) provides a stable voltage for ADC and comparison.

## 3.25 I2C bus

One I2C bus interface can work as a master or as a slave and support standard (up to 100 kbit/s), fast mode (up to 400 kbit/s) and fast mode plus (up to 1Mbit/s). It can output 15 mA driven current.

The I2C provides SMBus V2.0/PMBus 1.1 hardware support for: address resolution protocol (ARP) capability, host notification protocol, packet error checking (PEC) generation/verification, timeout verification and ALERT protocol management.

I2C can use a clock independent from the CPU clock domain to wake up MCU from Stop mode when I2C addresses match.

Table 3-3 I2C features

I2C features	I2C1
Master/Slave mode	Supported
Multiple master mode	Supported
Standard mode/Fast mode/Fast mode plus	Supported
7/10-bit addressing mode	Supported
Broadcast	Supported
Event management	Supported
Clock extend	Supported
Software reset	Supported
DMA transmission	Supported
Digital/analog filter	Supported
SMBUS2.0	Supported
PMBUS1.1	Supported
Independent clock	Supported
Wakeup from Stop mode	Supported

## 3.26 UART

HK32APIN02x embeds 6 universal asynchronous receiver and transmitter (UART1/2/3/4/5/6). The transmission rate is up to 10 Mbit/s. These interfaces provide asynchronous communication, multi-processor communication, single-wire half-duplex communication and have LIN Master/Slave capability.

All the USART interfaces provide hardware management of the CTS, RTS and RS485 DE signals, multiple processor communication mode, single-wire half-duplex communication mode.

UART can be served by DMA.

Table 3-4 UART1 features

Features	UART1/2/3/4/5/6
Data length	7/8/9-bit
DMA continuous transmission	Yes (except for UART5)
Multi-processor communication	Yes
Single-wire half-duplex communication	Yes
RS232 hardware flow control	Yes
RS485 driver enable	Yes

### 3.27 SPI

HK32APIN02x has 1 SPI interface. The master or slave mode, full-duplex and half-duplex communication mode are supported. The 3-bit prescaler gives 8 master mode frequencies. Each frame can be configured to 8 or 16 bits.

Table 3-5 SPI features

SPI features	SPI 1
Hardware CRC computation	Yes
RX/TX FIFO	Yes
NSS pulse mode	Yes
TI mode	Yes
DMA transmission	Yes

### 3.28 CAN

HK32APIN02x has an independent CAN interface. The CAN interface is compliant with Specification 2.0A and 2.0B (active). It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has 3 transmit mailboxes and 2 receive FIFOs with 3 stages 14 scalable filter banks.

### 3.29 96-bit UID

A 96-bit unique identification (UID) provides a reference number corresponding to each HK32ASPIN02x SOC. Under any circumstance, the UID is unique. You are prohibited to modify the UID. Depending on different applications, the 96-bit UID can be read in unit of byte (8 bits), half-word (16 bits) or word (32 bits). The 96-bit UID is suitable for the following applications:

- As a part number (for example, as a USB character serial number or other terminal applications).
- As a keyword. When programming the Flash, use the UID together with software encryption and decryption algorithm to enhance the security of the code in the Flash.
- Activating the boot process of the security mechanism.

### 3.30 Debug Interface

Build-in ARM SWJ-DP interface, which combined with a single wire debug interface, to realize the connection between serial single wire debug interfaces (SWDIO and SWCLK).

## 4 Electrical characteristics

### 4.1 Absolute maximum values

Note:

- Stresses above the absolute maximum rating listed in [Table 4-1](#) and [Table 4-31](#) may cause permanent damage to the device.
- Exposure to maximum permitted conditions for extended periods may affect device reliability.

#### 4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD-VSS}$	External main supply voltage (including $V_{DDA}$ and $V_{DD}$ )	-0.3	5.8	V
$V_{IN}$	Input voltage on pins	-0.3	5.8	
$ V_{SSX} - V_{SS} $	Variation between different $V_{DD}$ ground pins		50	mV

#### 4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
$I_{VDD}$	Total current into $V_{DD}/V_{DDA}$ power lines (source) <sup>(1)</sup>	105	mA
$I_{VSS}$	Total current out of $V_{SS}$ ground lines (sink) <sup>(1)</sup>	105	
$I_{IO}$	Output current sunk by any I/O and control pin	16	
	Output current source by any I/O and control pin	16	
$I_{INJ(PIN)}^{(2)}$	Injected current on pins <sup>(3)</sup>	-5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pin) <sup>(4)</sup>	-25/+0	

- (1). All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and Ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
- (2). Negative injected current disturbs the analog performance of the device.
- (3). When  $V_{IN} > V_{DD}$ , a positive injected current is induced. When  $V_{IN} < V_{SS}$ , a negative injected current is induced, and the injected current must be limited to the permitted range.
- (4). When several I/Os are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

#### 4.1.3 Thermal characteristics

Table 4-3 Thermal characteristics

Symbol	Description	Min	Max	Unit
$T_{STG}$	Storage temperature range	-55	130	°C
$T_J$	Maximum junction temperature	-45	110	

## 4.2 Operation conditions

### 4.2.1 General operation conditions

Table 4-4 General operation conditions

Symbol	Description	Min	Max	Unit
f <sub>HCLK</sub>	Internal AHB clock frequency	-	80	MHz
f <sub>PCLK1</sub>	Internal APB1 clock frequency	-	80	
f <sub>PCLK2</sub>	Internal APB2 clock frequency	-	80	
V <sub>DD</sub>	Standard operating voltage	2.2	5.5	V
V <sub>DDA</sub> <sup>(1)</sup>	Analog operating voltage	2.2	5.5	V
T	Operating temperature	-40	105	°C

(1). V<sub>DDA</sub> can be lower than V<sub>DD</sub>, for example, V<sub>DD</sub>=4.2V, V<sub>DDA</sub>=3.3V; V<sub>DD</sub>=3.3V, V<sub>DDA</sub>=2.5V.

### 4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Description	Threshold	Min	Typ	Max	Unit
V <sub>PVD</sub>	PVD thresholds (V <sub>DD</sub> rising edge) (-40°C ~105°C)	V <sub>PVD2</sub>	2.201	2.443	2.652	V
		V <sub>PVD3</sub>	2.383	2.641	2.852	
		V <sub>PVD4</sub>	2.582	2.841	3.052	
		V <sub>PVD5</sub>	2.761	3.036	3.252	
		V <sub>PVD6</sub>	2.940	3.220	3.453	
		V <sub>PVD7</sub>	3.122	3.405	3.652	
		V <sub>PVD8</sub>	3.279	3.586	3.852	
		V <sub>PVD9</sub>	3.462	3.783	4.050	
		V <sub>PVD10</sub>	3.643	3.975	4.252	
		V <sub>PVD11</sub>	3.820	4.161	4.452	
		V <sub>PVD12</sub>	4.021	4.375	4.650	
		V <sub>PVD13</sub>	4.221	4.565	4.851	
		V <sub>PVD14</sub>	4.381	4.744	5.003	
		V <sub>PVD15</sub>	4.558	4.925	5.153	
		PVD thresholds (V <sub>DD</sub> falling edge) (-40°C ~105°C)	V <sub>PVD2</sub>	2.097	2.288	
	V <sub>PVD3</sub>		2.257	2.482	2.697	
	V <sub>PVD4</sub>		2.439	2.674	2.895	
	V <sub>PVD5</sub>		2.636	2.862	3.098	
	V <sub>PVD6</sub>		2.798	3.057	3.296	
	V <sub>PVD7</sub>		2.998	3.253	3.498	
	V <sub>PVD8</sub>		3.179	3.453	3.697	
	V <sub>PVD9</sub>		3.358	3.642	3.899	
	V <sub>PVD10</sub>		3.538	3.841	4.097	
	V <sub>PVD11</sub>		3.736	4.043	4.297	
	V <sub>PVD12</sub>		3.917	4.236	4.497	
	V <sub>PVD13</sub>	4.099	4.432	4.698		

Symbol	Description	Threshold	Min	Typ	Max	Unit
		V <sub>VPD14</sub>	4.297	4.634	4.896	
		V <sub>VPD15</sub>	4.479	4.827	5.053	

### 4.2.3 BOR characteristics

Table 4-6 BOR characteristics

Symbol	Description	Threshold	Min	Typ	Max	Unit
V <sub>BOR</sub> <sup>(1)</sup>	BOR thresholds (V <sub>DD</sub> rising edge) (-40°C ~105°C)	V <sub>BOR2</sub>	2.099	2.287	2.352	V
		V <sub>BOR3</sub>	2.352	2.467	2.550	
		V <sub>BOR4</sub>	2.550	2.665	2.752	
		V <sub>BOR5</sub>	2.702	2.860	2.951	
		V <sub>BOR6</sub>	2.902	3.052	3.150	
		V <sub>BOR7</sub>	3.100	3.251	3.353	
		V <sub>BOR8</sub>	3.303	3.460	3.552	
		V <sub>BOR9</sub>	3.451	3.646	3.752	
		V <sub>BOR10</sub>	3.651	3.839	3.952	
		V <sub>BOR11</sub>	3.851	4.042	4.152	
		V <sub>BOR12</sub>	4.049	4.244	4.352	
		V <sub>BOR13</sub>	4.200	4.437	4.552	
		V <sub>BOR14</sub>	4.402	4.647	4.801	
		V <sub>BOR15</sub>	4.646	4.817	4.897	
		BOR thresholds (V <sub>DD</sub> falling edge) (-40°C ~105°C)	V <sub>BOR2</sub>	2.096	2.221	
	V <sub>BOR3</sub>		2.246	2.409	2.498	
	V <sub>BOR4</sub>		2.447	2.601	2.698	
	V <sub>BOR5</sub>		2.595	2.786	2.897	
	V <sub>BOR6</sub>		2.797	2.969	3.096	
	V <sub>BOR7</sub>		2.997	3.164	3.298	
	V <sub>BOR8</sub>		3.198	3.373	3.496	
	V <sub>BOR9</sub>		3.295	3.564	3.696	
	V <sub>BOR10</sub>		3.494	3.746	3.897	
	V <sub>BOR11</sub>		3.747	3.957	4.095	
	V <sub>BOR12</sub>		3.946	4.162	4.295	
	V <sub>BOR13</sub>		4.095	4.364	4.547	
	V <sub>BOR14</sub>	4.294	4.567	4.746		
V <sub>BOR15</sub>	4.646	4.817	4.897			
V <sub>BORhyst</sub>	BOR hysteresis	-	60	77	93	mV
t <sub>BORRST</sub> <sup>(2)</sup>	Onset time	-	-	50	-	μs

(1) BOR monitors V<sub>DD</sub> only.

(2) Design guarantees.

## 4.2.4 POR/PDR characteristics

Table 4-7 POR/PDR characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
V <sub>POR/PDR</sub> <sup>(1)</sup>	POR/PDR thresholds	Falling edge	1.899	2.006	2.104	V
		Rising edge	1.920	2.026	2.141	V
V <sub>PDRhyst</sub>	PDR hysteresis	-	0	21	45	mV
t <sub>RSTTEMPO</sub> <sup>(2)</sup>	Reset time	-	-	4	-	ms

(1) POR/PDR monitor V<sub>DD</sub> only.

(2) Design guarantees.

## 4.2.5 VREFINT characteristics

Table 4-8 VREFINT characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V <sub>REFINT</sub>	Internal reference voltage	-40 ~ 105°C	-	1.2	-	V

## 4.2.6 Operating current

Table 4-9 Operating current characteristics

Mode	Conditions	Parameter	V <sub>DD</sub> =3.3V			Unit
			-40° C	25° C	105° C	
Run mode	HSI=8MHz, V <sub>DD</sub> =3.3V, APB Bus off	Operating current	1.773	1.818	1.867	mA
Sleep mode	LSI=32.768KHz, V <sub>DD</sub> =3.3V, APB Bus off	Operating current	344	364	399	μA
		Wakeup time	-	29.8	-	μs
Stop mode	V <sub>DD</sub> =3.3V	Operating current	340	361	395	μA
		Wakeup time	-	33	-	μs

## 4.2.7 HSE clock characteristics

Table 4-10 HSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f <sub>OSC_IN</sub>	Oscillator frequency	-	4	-	24	MHz
R <sub>F</sub> <sup>(1)</sup>	Feedback resistor	-	-	2	-	MΩ
T <sub>stb (HSE)</sub> <sup>(2)</sup>	Oscillator start-up time	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-	2	-	ms
C	Equivalent series capacitor (recommended load capacitance deduct R <sub>S</sub> )	-	-	12	-	pF
I <sub>DD (HSE)</sub> <sup>(1)</sup>	HSE oscillator power consumption	Run mode: V <sub>DD</sub> =3.3V, CL=12pF	20	-	140	μA

(1) Design guarantees.

(2) T<sub>stb (HSE)</sub> is the time interval from HSE oscillator starts to it exports steady frequency signal.

HK32APIN02x integrates a HSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

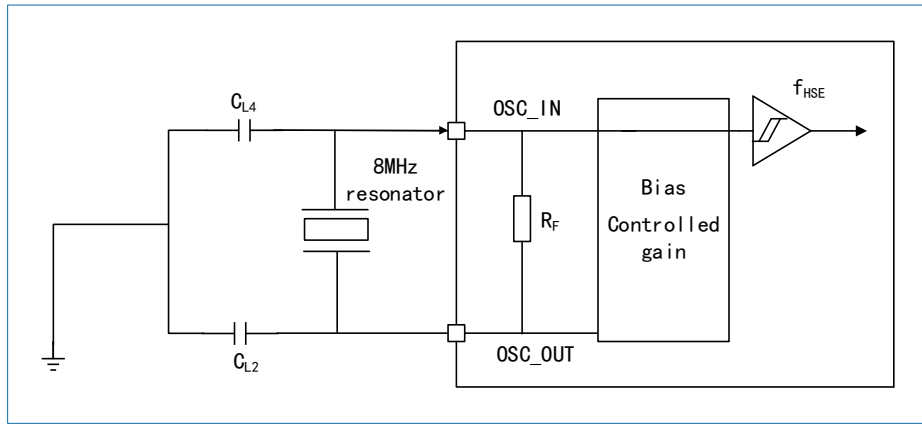


Figure 4-1 Typical application with an 8 MHz crystal

HK32APIN02x can also be clocked from the OSC\_IN pin (HSE\_ext). The requirements of this clock signal are described as follows:

Table 4-11 High-speed external user clock input characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$f_{HSE\_ext}$	External user clock frequency	-	-	-	30	MHz
$DuCy_{(HSE)}^{(1)}$	Duty cycle	-	45	-	55	%

## 4.2.8 LSE clock characteristics

Table 4-12 LSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$R_F^{(1)}$	Feedback resistor	-	-	10	-	MΩ
$T_{stb(LSE)}^{(2)}$	Oscillator start-up time	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	2000	-	ms
C	Equivalent series capacitor (recommended load capacitance deduct $R_S$ )	-	-	12	-	pF
$I_{DD(LSE)}^{(1)}$	LSE oscillator power consumption	Run mode: $V_{DD}=3.3V, CL=12pF$	-	150	-	nA

(1) Design guarantees.

(2)  $T_{stb(LSE)}$  is the time interval from HSE oscillator starts to it exports steady frequency signal.

HK32APIN02x integrates an LSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

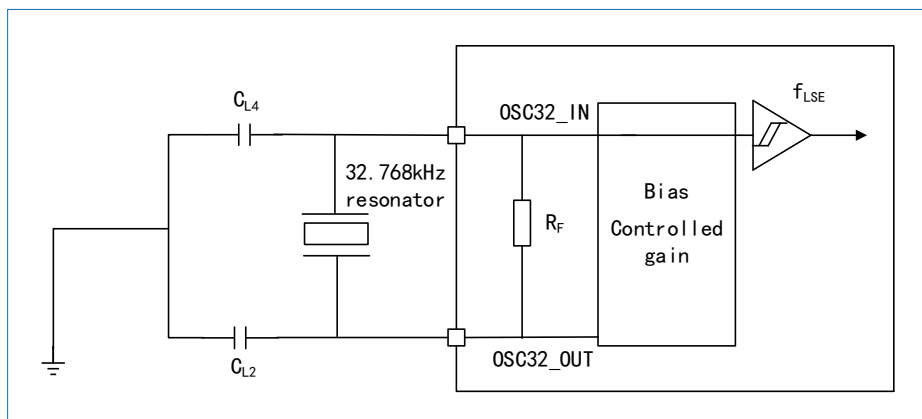


Figure 4-2 Typical application with LSE

HK32APIN02x supports the clock signal input from OSC32\_IN pin (LSE\_ext). The requirements of this clock signal are described as follows:

 Table 4-13 Low-speed external user clock input characteristics<sup>(1)</sup>

Symbol	Description	Conditions	Min	Typ	Max	Unit
f <sub>LSE_ext</sub>	external user clock frequency	-	-	32.768	-	MHz
DuCy <sub>(HSE)</sub>	Duty cycle	-	45	-	55	%

(1) Design guarantees.

## 4.2.9 High-speed internal (HSI) RC oscillator

Table 4-14 HSI RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f <sub>HSI</sub>	Frequency	-	-	8	-	MHz
DuCy <sub>(HSI)</sub> <sup>(1)</sup>	Duty cycle	-	45	-	55	%
ACC <sub>(HSI)</sub>	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register	-1	-	1	
		Factory calibrated TA= -40 ~ +105°C	-1	0.7	2.5	%
T <sub>stb(HSI)</sub> <sup>(1)</sup>	HSI oscillator startup time	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-	5	10	μs
ID <sub>D(HSI)</sub> <sup>(1)</sup>	HSI oscillator power consumption	8MHz, V <sub>DD</sub> =3.3V	-	81	101	μA

(1) Design guarantees.

## 4.2.10 Low-speed internal (LSI) RC oscillator

Table 4-15 LSI RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f <sub>LSI</sub>	Frequency	-	-	32.768	-	kHz
T <sub>su(LSI)</sub> <sup>(1)</sup>	LSI oscillator startup time	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-	120	240	μs
I <sub>DD(LSI)</sub> <sup>(1)</sup>	LSI oscillator power consumption	-	-	500	-	μA

(1) Design guarantees.

## 4.2.11 PLL characteristics

 Table 4-16 PLL characteristics<sup>(1)</sup>

Symbol	Description	Value			Unit
		Min	Typ	Max	
f <sub>PLL_IN</sub>	PLL Input clock	2	5	30	MHz
	PLL input clock duty	45	-	55	%
f <sub>PLL_OUT</sub>	PLL multiplier output clock	30	-	80	MHz
t <sub>LOCK</sub>	PLL Lock time	-	50	100	μs

(1) Design guarantees.

## 4.2.12 Flash memory characteristics

Table 4-17 Flash memory characteristics

Symbol	Description	Min	Typ <sup>(1)</sup>	Max	Unit
T <sub>PROG</sub>	A word programming time	73	73	76	μs
T <sub>ERASE</sub>	Page erase time	4.056	4.056	5.056	ms
	Mass erase time	486.72	486.72	606.72	ms
I <sub>DDPROG</sub>	programming current	-	-	3.5	mA
I <sub>DDERASE</sub>	Page/mass erase time	-	-	2	mA
I <sub>DDREAD</sub>	Supply current (read mode)	0.2(1MHZ)	3(40MHZ)	4.5(40MHZ)	mA
N <sub>END</sub>	Endurance	20	-	-	kcycles
t <sub>RET</sub>	Data retention	100(25°C)	-	-	year

(1) Typical value is obtained under 1.5V TT at 25°C.

## 4.2.13 I/O port input characteristics

Table 4-18 I/O static characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	Input high level voltage	V <sub>DD</sub> =2.2V~5.5V	0.42*(V <sub>DD</sub> -2)+1	-	5.5	V
V <sub>IL</sub>	Input low level voltage	V <sub>DD</sub> =2.2V~5.5V	-0.3	-	0.32*(V <sub>DD</sub> -2)+0.75	V
V <sub>IHhys</sub>	Input high level voltage	V <sub>DD</sub> =5.5V	2.6	-	-	V
V <sub>ILhys</sub>	Input low level voltage	V <sub>DD</sub> =5.5V	-	-	2.3	V
V <sub>hys</sub>	Schmitt trigger voltage hysteresis	V <sub>DD</sub> =2.2V~5.5V	5%*V <sub>DD</sub> <sup>(2)</sup>	-	-	mV
I <sub>lkg</sub>	Input leakage current	V <sub>DD</sub> =2.2V~5.5V V <sub>IN</sub> =5V	-	-	3	μA
R <sub>PU</sub>	Pull-up resistor	V <sub>IN</sub> =V <sub>SS</sub>	30	40	50	KΩ
R <sub>PD</sub>	Pull-down resistor	V <sub>IN</sub> =V <sub>DD</sub>	30	40	50	KΩ
C <sub>IO</sub> <sup>(1)</sup>	I/O pin capacitance	-	-	5	-	pF

(1) Design guarantees.

(2) Minimum value is 100mV.

## 4.2.14 I/O port output characteristics

Table 4-19 Output voltage DC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V <sub>OH</sub>	Output high level voltage	2.2 V ≤ V <sub>DD</sub> ≤ 5.5 V	V <sub>DD</sub> -0.5	-	-	V
V <sub>OL</sub>	Output low level voltage	2.2 V ≤ V <sub>DD</sub> ≤ 5.5 V	-	-	0.5	V

Table 4-20 Output voltage AC characteristics

Mode	Symbol	Description	Conditions	Min	Typ	Max	Unit
OSPEEDy [1:0]							
x0	t <sub>f(I/O)out</sub>	Output fall time	CL = 50 pF, V <sub>DD</sub> = 2.2V~5.5V	-	-	105	ns
	t <sub>r(I/O)out</sub>	Output rise time		-	-	105	ns

Mode	Symbol	Description	Conditions	Min	Typ	Max	Unit
OSPEEDy [1:0]							
01	$t_{f(I/O)out}$	Output fall time	CL = 50 pF,	-	-	25	ns
	$t_{r(I/O)out}$	Output rise time	$V_{DD} = 2.2V \sim 5.5V$	-	-	25	ns
11	$t_{f(I/O)out}$	Output fall time	CL = 50 pF,	-	-	8	ns
	$t_{r(I/O)out}$	Output rise time	$V_{DD} = 2.2V \sim 5.5V$	-	-	8	ns

#### 4.2.15 NRST reset pin characteristics

NRST pin is integrated with inner a pull-up resistor, it can be connected with external RC circuit, or without any circuit.

Table 4-21 NRST pin input characteristics

Symbol	Description	Min	Max	Unit
$T_{Noise}$	Ignore time of low level voltage	-	80	ns

#### 4.2.16 TIM timer characteristics

Table 4-22 TIM characteristics

Symbol	Description	Min	Max	Unit
$F_{EXT}$	Timer external clock frequency on CH1 to CH4	-	40	MHz

(1).  $f_{TIM \times CLK} = 80 \text{ MHz}$

#### 4.2.17 EMACC characteristics

Table 4-23 Frequency characteristics of motor-drive

SYSCLK frequency	ADC Clock frequency	Min	Typ	Max	Unit
80 MHz	$f_{PCLK} = f_{apb}$ $f_{ADC} = f_{PCLK}/4$	-	20	25	kHz

Table 4-24 Efficiency comparison of FOC key algorithm with EMACC and software library

Test condition	Angle ( $\theta$ )	Coordinate system conversion	SVPWM	Total time consumption	Unit
SYSCLK: 80 MHz (software library)	11.6	10	4.8	28.8	$\mu s$
SYSCLK: 80 MHz (EMACC)	11.6	1.6	2.4	18	$\mu s$

#### 4.2.18 ADC characteristics

Table 4-25 ADC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{DDA}$	ADC power supply	-	2.2	3.3	5.5	V
$V_{REFP}$	Positive reference voltage	-	2.2	3.3	5.5	V
$V_{REFN}$	Negative reference voltage	-	0	0	0.1	V
$f_{ADC}$	ADC clock frequency	-	0.3	14	42	MHz
$f_s^{(1)}$	Sampling frequency	$f_{ADC} = 14 \text{ MHz}$	-	1	-	MHz
$f_{TRIG}^{(1)}$	External trigger frequency	$f_{ADC} = 14 \text{ MHz}$	-	-	823	kHz

Symbol	Description	Conditions	Min	Typ	Max	Unit
			17	-	-	Cycles
V <sub>AIN</sub>	Conversion voltage range	-	VREFN	-	VREFP	V
R <sub>AIN</sub> <sup>(1)</sup>	External input impedance	Please refer to Table 4-26				kΩ
R <sub>ADC</sub> <sup>(1)</sup>	Sampling switch resistance	-	-	-	1	kΩ
C <sub>ADC</sub> <sup>(1)</sup>	Internal sample and hold capacitor	-	-	5	-	pF
Jitter <sub>ADC</sub>	ADC trigger conversion jitter	-	-	1	-	Cycles
t <sub>S</sub> <sup>(1)</sup>	Sampling rate	f <sub>ADC</sub> = 14 MHz	-	1.5	-	Cycles
t <sub>CONV</sub> <sup>(1)</sup>	Total conversion time (including sampling time)	f <sub>ADC</sub> = 14 MHz, 12-bit resolution	-	14	-	Cycles

(1) Design guarantees.

The max input impedance R<sub>AIN</sub> must meet the following formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

N represents resolution, its value is 12.

Errors below 1/4 LSB (Least Significant Bit, LSB) is allowed.

Table 4-26 Max value of input impedance (f<sub>ADC</sub> = 14 MHz)

Sampling period (Cycles)	Sampling time (t <sub>S</sub> , μs)	Max input impedance (kΩ)
1.5	0.11	1.21
7.5	0.54	10.04
13.5	0.96	18.87
28.5	2.04	40.96
41.5	2.96	60.09
55.5	3.96	80.70
71.5	5.11	104.26
239.5	17.11	351.58

Table 4-27 ADC resolution

Symbol	Parameter	Description	Conditions	Typ	Max	Unit
ET	Total unadjusted error <sup>(1)</sup>	maximum deviation between the actual and the idea transfer curves	V <sub>DD</sub> =V <sub>DDA</sub> =3.3V, f <sub>ADC</sub> = 14 MHz, Measurements made after ADC calibration	-	15	LSB
EO	Offset error <sup>(2)</sup>	deviation between the first actual and the first idea transfer curves		-	14	
EG	Gain error <sup>(3)</sup>	-		-	5	
ED	Differential linearity error <sup>(4)</sup>	-		-	1	
EL	Integral linearity error <sup>(5)</sup>	-		-	1	

(1) Total unadjusted error: maximum deviation between the actual and the idea transfer curves.

(2) Offset error: deviation between the first actual and the first idea transfer curves.

(3) Gain error: deviation between the last actual and the last idea transfer curves.

(4) Differential linearity error: maximum deviation between actual steps and the idea one.

(5) Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Note:

- ADC DC accuracy values are measured after internal calibration.
- ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
- Better performance could be achieved in restricted  $V_{DD}$ , frequency,  $V_{REF}$  and temperature ranges.
- Based on characterization, not tested in production.

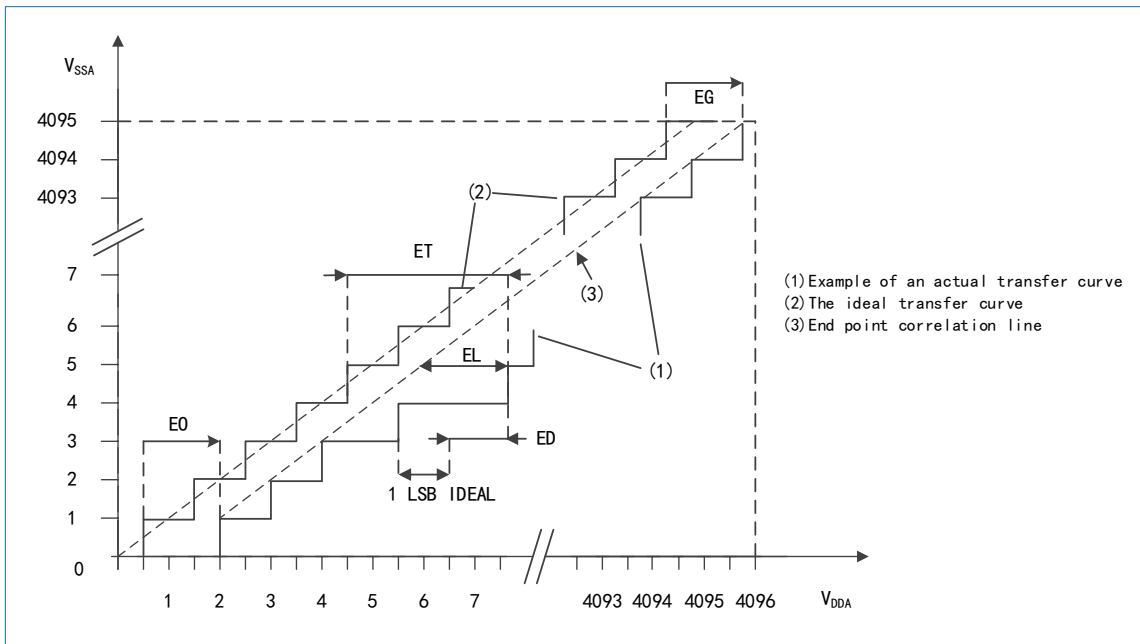


Figure 4-3 ADC accuracy characteristics

Note: Please refer to [Table 4-27](#) for detail information of EO, ET, EG, EL, and ED.

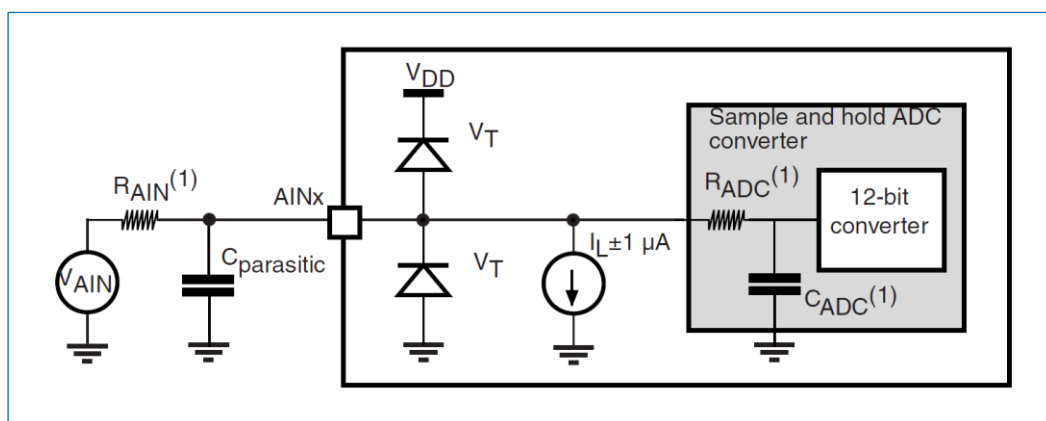


Figure 4-4 Typical connection diagram using the ADC

(1). Refer to [Table 4-25](#) for the values of  $R_{ADC}$  and  $C_{ADC}$ .

$C_{parasitic}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high  $C_{parasitic}$  value will downgrade conversion accuracy. To remedy this,  $f_{ADC}$  should be reduced.

General PCB design guidelines:

Power supply decoupling should be performed as show in [Figure 5-1](#). The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

#### 4.2.19 Temperature sensor characteristics

Table 4-28 Temperature sensor characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
T <sub>L</sub>	V <sub>SENSE</sub> linearity with temperature	-20°C~70°C	-	-	±3	°C
		-40°C~105°C	-	-	±6	
V <sub>20</sub>	Output voltage	20°C	-	936.6	-	mV
Avg_Slope	Average slope	-	-	2.87	-	mV/°C

#### 4.2.20 DAC voltage divider characteristics

Table 4-29 DAC voltage divider characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V <sub>DDA</sub>	Analog supply voltage	DAC on	1.8	5	5.5	V
R <sub>o</sub>	Impedance output	DAC buffer on	-	7	-	kΩ
I <sub>OUT</sub> <sup>(1)</sup>	Current output	DAC buffer off	-	-	2	mA

#### 4.2.21 COMP characteristics

Table 4-30 COMP characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V <sub>DDA</sub>	Analog supply voltage	-	2.2	5	5.5	V
V <sub>com</sub>	Input common-mode voltage	-	-0.3	-	5.5	V
V <sub>diff</sub>	Input differential-mode voltage	V <sub>DDA</sub> =5V, V <sub>com</sub> =2.5V, no hysteresis	5	-	-	mV
V <sub>hy</sub>	Hysteresis voltage	Threshold 1	-	0	-	mV
		Threshold 2	-	30	-	
		Threshold 3	-	60	-	
		Threshold 4	-	100	-	
I <sub>OP</sub>	Operating voltage V <sub>DD</sub> =5V	Low power mode	-	1	-	μA
		High power mode	-	5.05	-	
T <sub>dly</sub> <sup>(1)</sup>	Output delay (No hysteresis)	High power mode Rising edge	37	-	86	ns
		Low power mode Rising edge	572	-	998	
		High power mode Falling edge	51	-	169	
		Low power mode Falling edge	327	-	1200	

(1) Design guarantees.

## 4.2.22 OPAMP characteristics

Table 4-31 OPAMP characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V <sub>DDA</sub>	Analog supply voltage	-	2.2	5	5.5	V
V <sub>OUT</sub>	Output voltage	-	0.2	-	V <sub>DDA</sub> -0.2	V
CMIR	Input common-mode voltage	-	0	-	5.5	V
I <sub>bias</sub> <sup>(1)</sup>	Input bias current	-	0.8	1	1.2	μA
I <sub>load</sub>	Output current	R <sub>L</sub> =100Ω, V <sub>DDA</sub> =5V	-	10	-	mA
I <sub>q</sub>	Operating current	No-load, static state	438	900	1700	μA
I <sub>l</sub> <sup>(1)</sup>	Leakage current	OPAMP off	-	3	275	nA
V <sub>os</sub>	Input bias voltage	Before calibration	-	±10	-	mV
		After calibration	-	-	±1.5	
CMRR	Common mode rejection ratio	-	51	-	145	dB
PSRR	Power supply rejection ratio	-	41	70	109.4	dB
GBW	bandwidth	-	5.83	10	22.91	MHz
SR	Slew rate	-	5.9	-	21	V/μs
φ	Phase margins	-	47	60	71.62	Deg
PGA gain	PGA gain	Threshold 1	-	2	-	times
		Threshold 2	-	4	-	
		Threshold 3	-	8	-	
		Threshold 4	-	16	-	

## 5 Power supply scheme

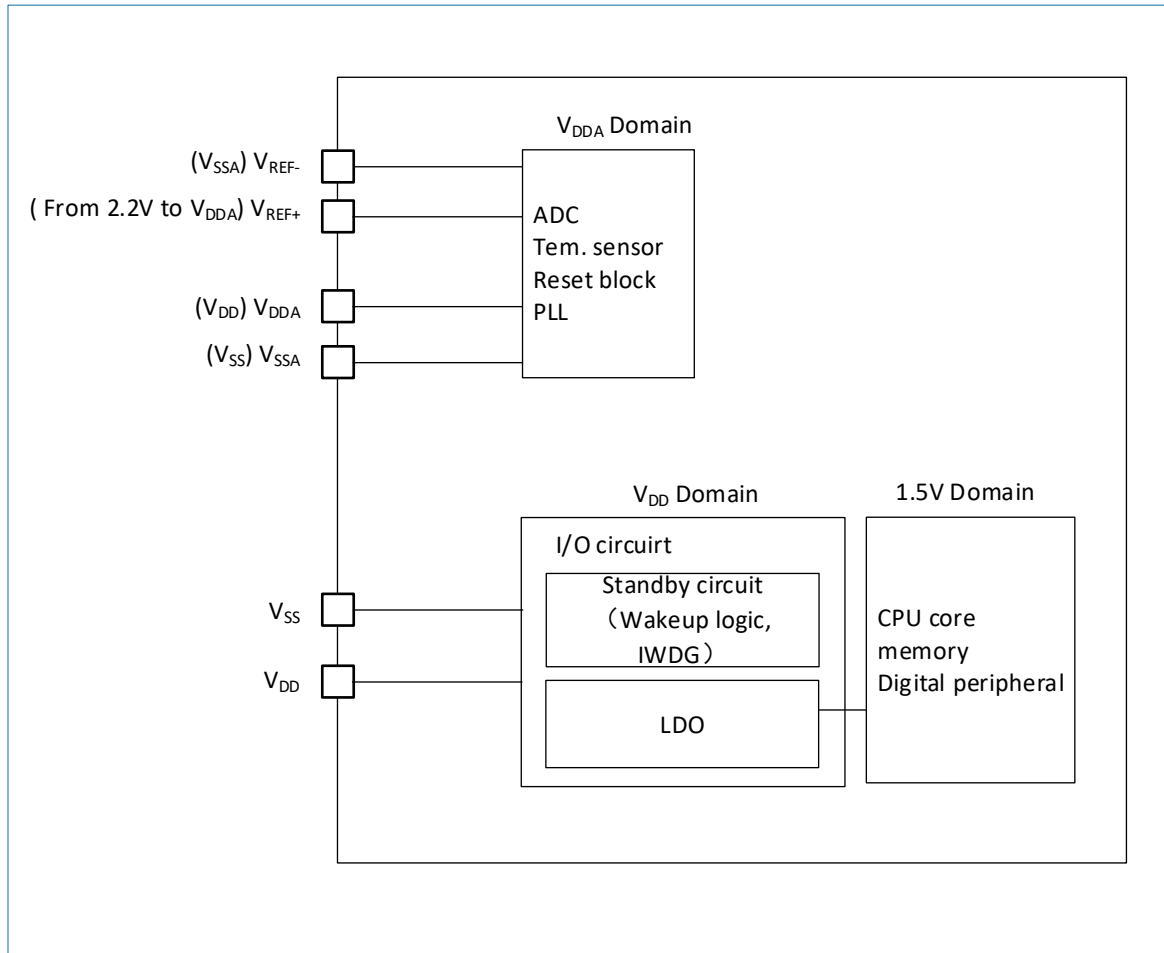


Figure 5-1 Power supply diagram

## 6 Pinouts and pin descriptions

HK32APIN02x provides four packages: LQFP48, LQFP44, LQFP32, TSSOP24.

## 6.1 LQFP48

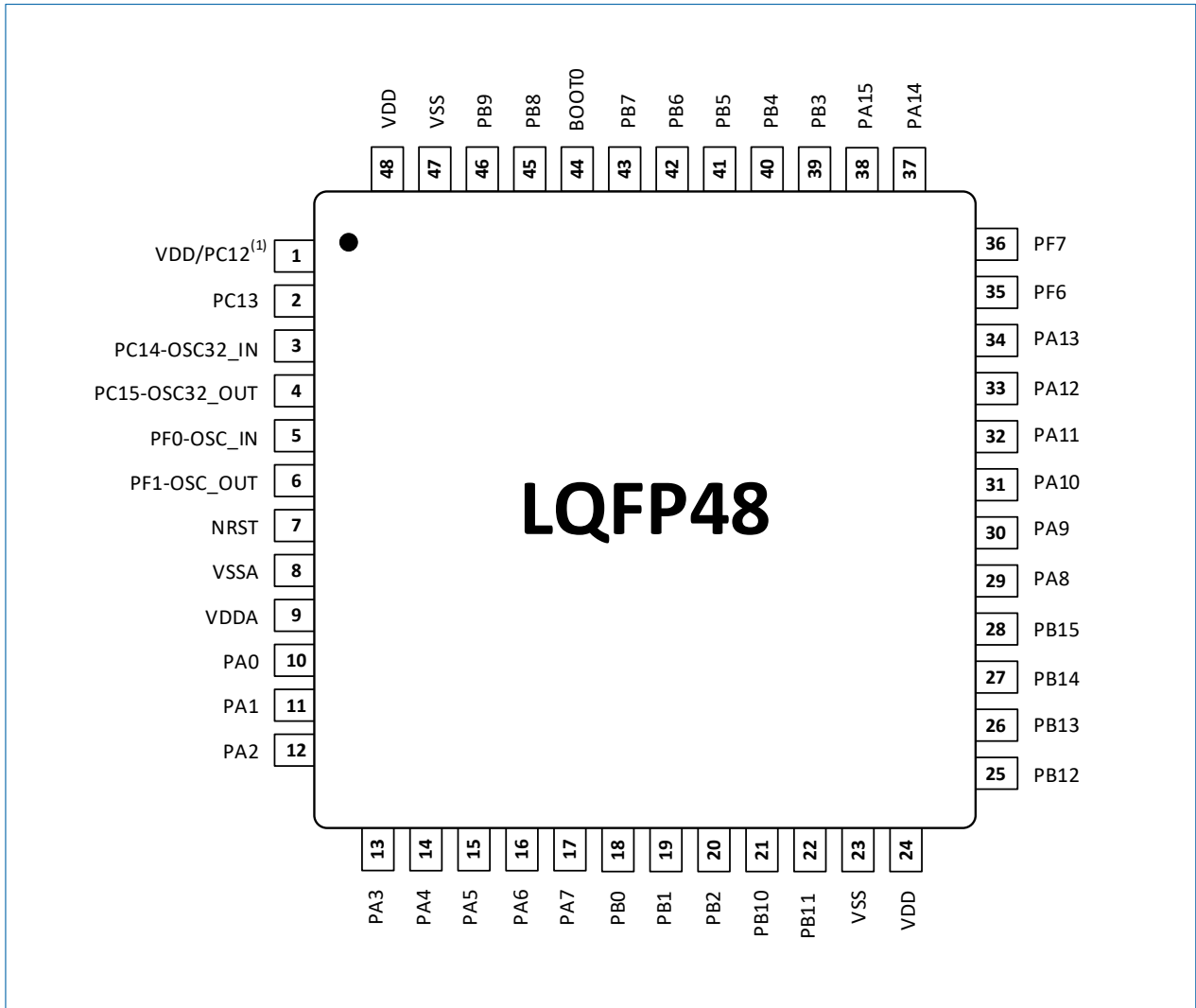


Figure 6-1 LQFP48 package pinout

Note of the above figure:

- (1). In HK32ASPIN021C8T7, this pin is PC12; in HK32ASPIN022C8T7, it is VDD.

## 6.2 LQFP44

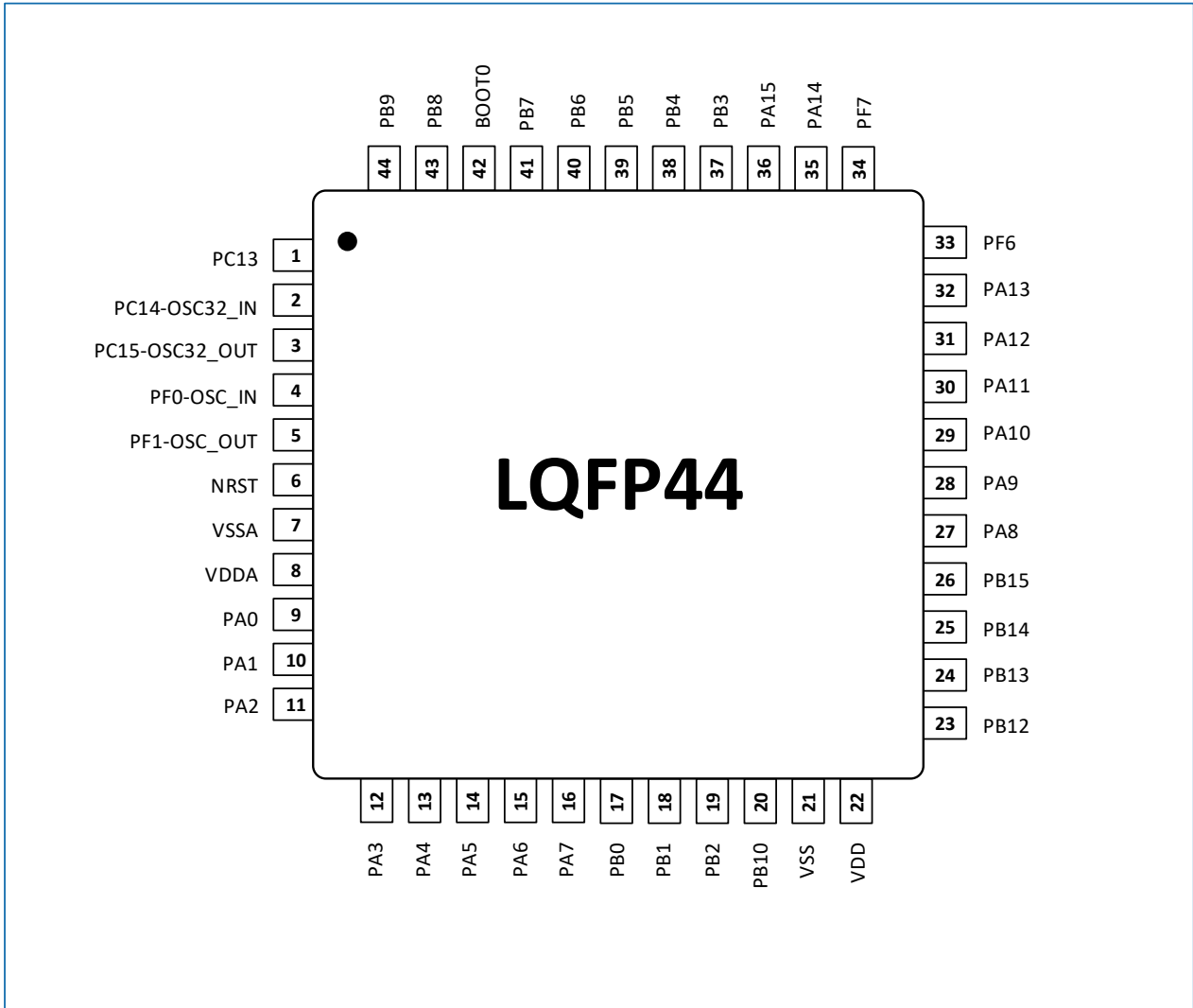


Figure 6-2 LQFP44 package pinout

### 6.3 LQFP32

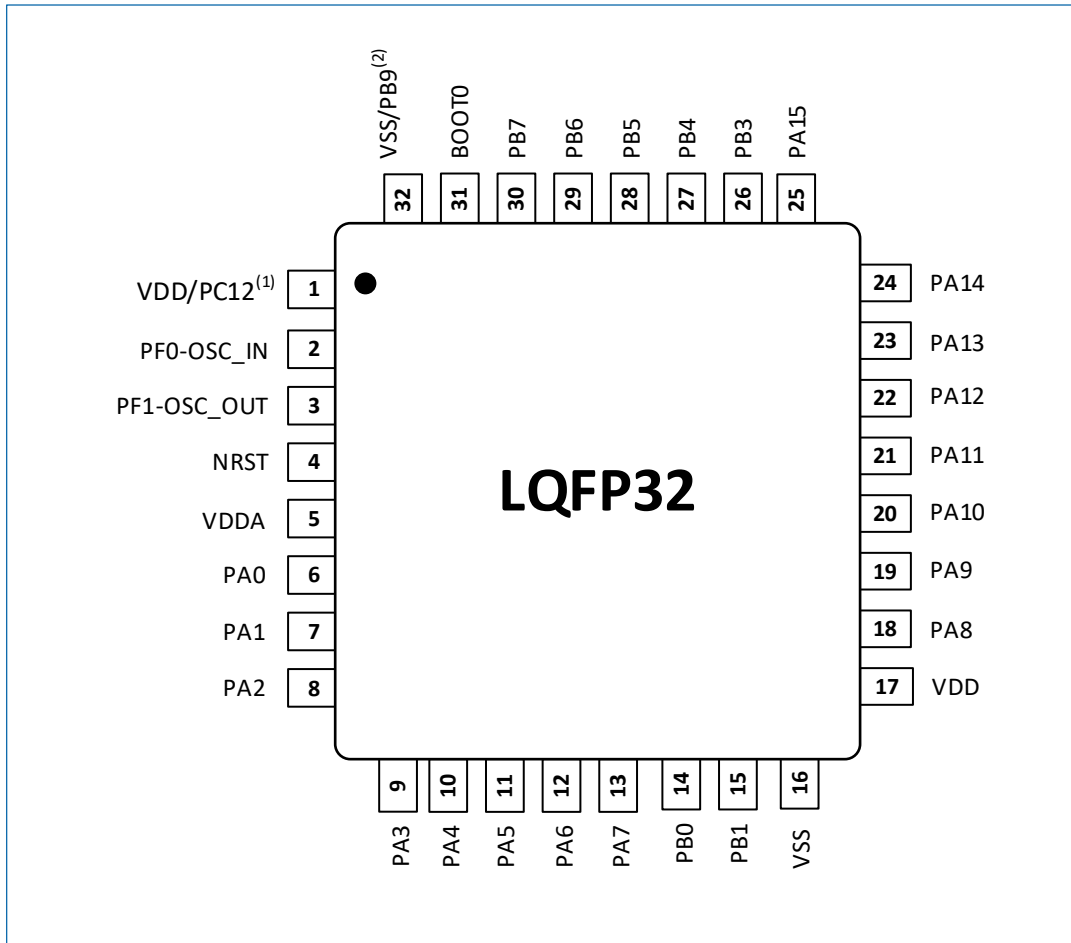


Figure 6-3 LQFP32 package pinout

Note for the above figure:

- (1). For HK32ASPIN020K8T7 and HK32ASPIN021K8T7, this pin is PC12, for HK32ASPIN022K8T7, it is VDD.
- (2). For HK32ASPIN020K8T7, this pin is PB9, for HK32ASPIN021K8T7 and HK32ASPIN022K8T7, it is VSS.

## 6.4 TSSOP24

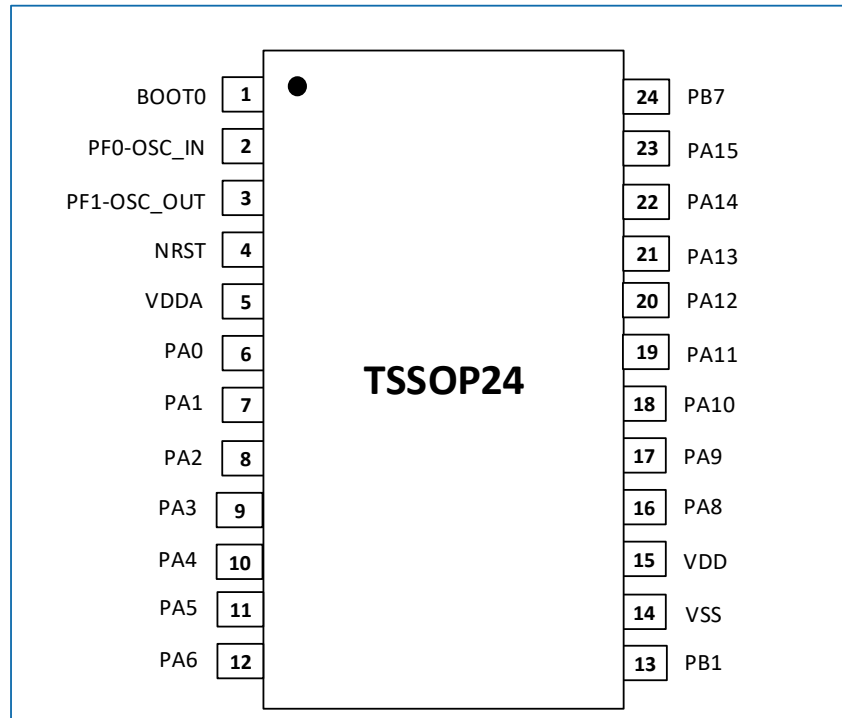


Figure 6-4 TSSOP20 package pinout

## 6.5 Pin description

Table 6-1 shows pin description of the four packages.

Table 6-1 HK32APIN02x pin descriptions

Pin number							Pin name (Default function after reset)	Pin type <sup>(1)</sup>	5V tolerant	Pin function	
LQFP48_1 <sup>(2)</sup>	LQFP48_2 <sup>(2)</sup>	LQFP44	LQFP32_1 <sup>(2)</sup>	LQFP32_2 <sup>(2)</sup>	LQFP32_3 <sup>(2)</sup>	TSSOP24				Alternate functions	Additional functions
-	1	-	-	-	1	-	VDD	S		Digital power supply	
1	-	-	1	1	-	-	PC12	I/O	FT	TIM1_ETR UART1_TX/UART1_RX UART3_TX/UART3_RX UART4_TX/UART4_RX UART5_TX/UART5_RX UART6_TX/UART6_RX TIM1_CH4	
2	2	1	-	-	-	-	PC13	I/O	FT	UART1_RX/UART1_TX UART2_RX/UART2_TX UART3_RX/UART3_TX UART4_RX/UART4_TX UART5_RX/UART5_TX UART6_RX/UART6_TX TIM1_BKIN	EXTIN13
3	3	2	-	-	-	-	PC14-OSC32_IN (PC14)	I/O	-	TIM2_ETR TIM2_CH1 UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX	OSC32_IN LSE_CKI EXTIN14

Pin number							Pin name (Default function after reset)	Pin type <sup>(1)</sup>	5V tolerant	Pin function	
LOFP48_1 <sup>(2)</sup>	LOFP48_2 <sup>(2)</sup>	LOFP44	LOFP32_1 <sup>(2)</sup>	LOFP32_2 <sup>(2)</sup>	LOFP32_3 <sup>(2)</sup>	TSS0P24				Alternate functions	Additional functions
										UART6_CTS TIM1_CH1	
4	4	3	-	-	-	-	PC15- OSC32_OUT (PC15)	I/O	-	TIM2_CH4 Trace_TX UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH1N	OSC32_OUT  EXTIN15
5	5	4	2	2	2	2	PF0-OSC_IN (PF0)	I/O	-	I2C1_SDA TIM2_CH1 TIM2_ETR UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH2	OSC_IN  HSE_CKI
6	6	5	3	3	3	3	PF1-OSC_OUT (PF1)	I/O	-	I2C1_SCL TIM2_CH2 Trace_TX UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH2N	OSC_OUT
7	7	6	4	4	4	4	NRST_PF9	I/O	FT	TIM2_CH3 UART1_TX/UART1_RX UART2_TX/UART2_RX UART3_TX/UART3_RX UART4_TX/UART4_RX UART5_TX/UART5_RX UART6_TX/UART6_RX TIM1_BKIN	EXTIN9
8	8	7	-	-	-		VSSA	S		Analog ground	
9	9	8	5	5	5	5	VDDA	S		Analog power supply	
10	10	9	6	6	6	6	PA0	I/O	-	TIM2_ETR TIM2_CH1 Trace_TX UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH3 CAN_RX	ADC_IN0 OAMP1_INP3 OAMP2_INP3 COMP1_INP1 CKI_4 EXTIN0
11	11	10	7	7	7	7	PA1	I/O	-	CM0_TXEV TIM2_CH2 TIM15_CH1N	ADC_IN1 OAMP1_OUT

Pin number							Pin name (Default function after reset)	Pin type <sup>(1)</sup>	5V tolerant	Pin function	
LOFP48_1 <sup>(2)</sup>	LOFP48_2 <sup>(2)</sup>	LOFP44	LOFP32_1 <sup>(2)</sup>	LOFP32_2 <sup>(2)</sup>	LOFP32_3 <sup>(2)</sup>	TSS0P24				Alternate functions	Additional functions
										COMP1_OUT UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3N CAN_TX	COMP1_INN1 EXTIN1
12	12	11	8	8	8	8	PA2	I/O	-	TIM15_CH1 TIM2_CH3 TIM1_ETR COMP2_OUT UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH4 CAN_RX	ADC_IN2 OAMP1_INN0 COMP2_INN1 EXTIN2
13	13	12	9	9	9	9	PA3	I/O	-	TIM15_CH2 TIM2_CH4 UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH1 CAN_TX	ADC_IN3 OAMP1_INP2 OAMP2_INP2 COMP2_INP1 EXTIN3
14	14	13	10	10	10	10	PA4	I/O	-	SPI1_NSS TIM14_CH1 UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH1N CAN_RX	ADC_IN4 OAMP1_INP1 OAMP2_INP1 COMP1_INN2 COMP2_INN2 COMP3_INP1 CKI_1 EXTIN4
15	15	14	11	11	11	11	PA5	I/O	-	SPI1_SCK TIM2_ETR TIM2_CH1 UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH2 CAN_TX	ADC_IN5 OAMP2_INN0 COMP1_INN3 COMP2_INN3 COMP3_INN3 EXTIN5
16	16	15	12	12	12	12	PA6	I/O	-	SPI1_MISO TIM3_CH1 TIM2_CH2 TIM16_CH1 CMO_TXEV	ADC_IN6 OAMP2_OUT EXTIN6

Pin number							Pin name (Default function after reset)	Pin type <sup>(1)</sup>	5V tolerant	Pin function	
L0FP48_1 <sup>(2)</sup>	L0FP48_2 <sup>(2)</sup>	L0FP44	L0FP32_1 <sup>(2)</sup>	L0FP32_2 <sup>(2)</sup>	L0FP32_3 <sup>(2)</sup>	TSS0P24				Alternate functions	Additional functions
										COMP1_OUT UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH2N CAN_RX	
17	17	16	13	13	13	-	PA7	I/O	-	SPI1_MOSI TIM3_CH2 RCC_MCO TIM2_CH3 TIM14_CH1 CM0_TXEV UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH3 CAN_TX	ADC_IN7 OAMP1_INP0 OAMP2_INP0 COMP1_INP2 COMP2_INP2 COMP3_INP2 EXTIN7
18	18	17	14	14	14	-	PB0	I/O	-	CM0_TXEV TIM3_CH3 TIM2_CH4 UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH3N	ADC_IN8 COMP3_INN2 EXTIN0
19	19	18	15	15	15	13	PB1	I/O	-	TIM14_CH1 TIM3_CH4 Trace_TX COMP2_OUT COMP3_OUT UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH1	ADC_IN9 COMP3_INN1 EXTIN1
20	20	19	-	-	-	-	PB2	I/O	-	TIM2_ETR TIM2_CH1 I2C1_SMBA UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH1N	ADC_IN10 OAMP1_INN1 COMP1_INP3 EXTIN2
21	21	20	-	-	-	-	PB10	I/O	-	I2C1_SCL TIM2_CH2	ADC_IN11 OAMP2_INN1

Pin number							Pin name (Default function after reset)	Pin type <sup>(1)</sup>	5V tolerant	Pin function	
LOFP48_1 <sup>(2)</sup>	LOFP48_2 <sup>(2)</sup>	LOFP44	LOFP32_1 <sup>(2)</sup>	LOFP32_2 <sup>(2)</sup>	LOFP32_3 <sup>(2)</sup>	TSS0P24				Alternate functions	Additional functions
										UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH2 CAN_RX	COMP2_INP3 EXTIN10
22	22	-	-	-	-	-	PB11	I/O	-	CM0_TXEV I2C1_SDA TIM2_CH3 UART1_RX/UART1_TX UART2_RX/UART2_TX UART3_RX/UART3_TX UART4_RX/UART4_TX UART5_RX/UART5_TX UART6_RX/UART6_TX TIM1_CH2N CAN_TX	ADC_IN12 COMP3_INP3 EXTIN11
23	23	21	16	16	16	14	VSS	S		Ground	
24	24	22	17	17	17	15	VDD	S		Digital power supply	
25	25	23	-	-	-	-	PB12	I/O	-	SPI1_NSS CM0_TXEV TIM2_CH1 TIM2_ETR TIM15_BKIN COMP1_OUT UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH3 CAN_RX	ADC_IN13 EXTIN12
26	26	24	-	-	-	-	PB13	I/O	-	SPI1_SCK TIM2_CH2 COMP2_OUT UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3N CAN_TX	EXTIN13
27	27	25	-	-	-	-	PB14	I/O	-	SPI1_MISO TIM15_CH1 TIM2_CH3 TIM1_ETR COMP3_OUT UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS	EXTIN14

Pin number							Pin name (Default function after reset)	Pin type <sup>(1)</sup>	5V tolerant	Pin function	
LOFP48_1 <sup>(2)</sup>	LOFP48_2 <sup>(2)</sup>	LOFP44	LOFP32_1 <sup>(2)</sup>	LOFP32_2 <sup>(2)</sup>	LOFP32_3 <sup>(2)</sup>	TSS0P24				Alternate functions	Additional functions
										UART6_TX/UART6_RX TIM1_CH4	
28	28	26	-	-	-	-	PB15	I/O	FT	SPI1_MOSI TIM15_CH2 TIM2_CH4 TIM15_CH1N UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_BKIN	EXTIN15
29	29	27	18	18	18	16	PA8	I/O	FT	RCC_MCO CM0_TXEV UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH1 CAN_RX	EXTIN8
30	30	28	19	19	19	17	PA9	I/O	FT	TIM15_BKIN TIM2_ETR TIM2_CH1 I2C1_SCL RCC_MCO UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH1N CAN_TX	EXTIN9
31	31	29	20	20	20	18	PA10	I/O	FT	EXT_TRIG TIM2_CH2 I2C1_SDA Trace_TX UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH2 CAN_RX	EXTIN10
32	32	30	21	21	21	19	PA11	I/O	FT	CM0_TXEV UART1_CTS TIM2_CH3 UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX	EXTIN11

Pin number							Pin name (Default function after reset)	Pin type <sup>(1)</sup>	5V tolerant	Pin function	
LOFP48_1 <sup>(2)</sup>	LOFP48_2 <sup>(2)</sup>	LOFP44	LOFP32_1 <sup>(2)</sup>	LOFP32_2 <sup>(2)</sup>	LOFP32_3 <sup>(2)</sup>	TSS0P24				Alternate functions	Additional functions
										TIM1_CH2N CAN_TX	
33	33	31	22	22	22	20	PA12	I/O	FT	CM0_TXEV TIM2_CH4 UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH3 CAN_RX	EXTIN12
34	34	32	23	23	23	21	PA13  (SWDIO)	I/O	FT	CM0_SWD IRTIM_IROUT EXT_TRIG UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3N	CKI_2 EXTIN13
35	35	33	-	-	-	-	PF6	I/O	FT	I2C1_SCL TIM1_ETR UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH4	EXTIN6
36	36	34	-	-	-	-	PF7	I/O	FT	I2C1_SDA EXT_TRIG UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_BKIN	EXTIN7
37	37	35	24	24	24	22	PA14  (SWCLK)	I/O	FT	CM0_SWCLK Trace_TX TIM1_ETR UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH4	CKI_3 EXTIN14
38	38	36	25	25	25	23	PA15	I/O	FT	SPI1_NSS TIM2_ETR TIM2_CH1 CM0_TXEV EXT_TRIG Trace_TX	EXTIN15

Pin number							Pin name (Default function after reset)	Pin type <sup>(1)</sup>	5V tolerant	Pin function	
LOFP48_1 <sup>(2)</sup>	LOFP48_2 <sup>(2)</sup>	LOFP44	LOFP32_1 <sup>(2)</sup>	LOFP32_2 <sup>(2)</sup>	LOFP32_3 <sup>(2)</sup>	TSS0P24				Alternate functions	Additional functions
										UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3N CAN_TX	
39	39	37	26	26	26	-	PB3	I/O	FT	SPI1_SCK CMO_TXEV TIM2_CH2 UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH1 CAN_RX	EXTIN3
40	40	38	27	27	27	-	PB4	I/O	FT	SPI1_MISO TIM3_CH1 CMO_TXEV TIM2_CH3 TIM3_ETR UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH1N CAN_TX	EXTIN4
41	41	39	28	28	28	-	PB5	I/O	FT	SPI1_MOSI TIM3_CH2 TIM16_BKIN I2C1_SMBA TIM2_CH4 UART1_TX/UART1_RX UART2_RX/UART2_TX UART3_TX/UART3_RX UART4_RX/UART4_TX UART5_TX/UART5_RX UART6_RX/UART6_TX TIM1_CH2 CAN_RX	EXTIN5
42	42	40	29	29	29	-	PB6	I/O	FT	I2C1_SCL TIM16_CH1N UART1_TX/UART1_RX UART2_CT UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH2N CAN_TX	EXTIN6
43	43	41	30	30	30	24	PB7	I/O	FT	I2C1_SDA TIM2_CH2	EXTIN7

Pin number							Pin name (Default function after reset)	Pin type <sup>(1)</sup>	5V tolerant	Pin function	
LOFP48_1 <sup>(2)</sup>	LOFP48_2 <sup>(2)</sup>	LOFP44	LOFP32_1 <sup>(2)</sup>	LOFP32_2 <sup>(2)</sup>	LOFP32_3 <sup>(2)</sup>	TSS0P24				Alternate functions	Additional functions
										EXT_TRIG COMP3_OUT UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3 CAN_RX	
44	44	42	31	31	31	-	BOOT0_PF8	I/O	FT	TIM2_CH3 TIM3_CH3 Trace_TX UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_R UART5_CTS UART6_TX/UART6_RX TIM1_CH3N	BOOT0
45	45	43	-	-	-	-	PB8	I/O	FT	I2C1_SCL TIM16_CH1 UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH3 CAN_RX	EXTIN8
46	46	44	32	-	-	-	PB9	I/O	FT	IRTIM_IROUT I2C1_SDA CM0_TXEV UART1_RX/UART1_TX UART2_TX/UART2_RX UART3_RX/UART3_TX UART4_TX/UART4_RX UART5_RX/UART5_TX UART6_TX/UART6_R TIM1_CH3N CAN_TX	EXTIN9
47	47	-	-	32	32	-	VSS	S		Ground	
48	48	-	-	-	-	-	VDD	S		Digital power supply	

(1). I= input, O=output, I/O= input/output, S=supply.

Note: Unless otherwise specified, all I/Os are set to float input in the process of reset or after reset.

## 6.6 AF function and pin mapping

Table 6-2 Pin Alternate Function

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0/A IN0		TIM2_ ETR	TIM2_ CH1			Trace_ TX			UART 1_TX/ UART 1_RX	UART 2_CTS	UART 3_TX/ UART 3_RX	UART 4_CTS	UART 5_TX/ UART 5_RX	UART6 _CTS	TIM1 _CH3	CAN _RX
PA1/A IN1	CM0_ TXEV		TIM2_ CH2			TIM15 _CH1 N		COMP 1_OU T	UART 1_RX/ UART 1_TX	UART 2_RTS	UART 3_RX/ UART 3_TX	UART 4_RTS	UART 5_RX/ UART 5_TX	UART6 _RTS	TIM1 _CH3 N	CAN _TX
PA2/A IN2	TIM1 5_CH 1		TIM2_ CH3				TIM1_ ETR	COMP 2_OU T	UART 1_CTS	UART 2_TX/ UART 2_RX	UART 3_CTS	UART 4_TX/ UART 4_RX	UART 5_CTS	UART6 _TX/U ART6_ RX	TIM1 _CH4	CAN _RX
PA3/A IN3	TIM1 5_CH 2		TIM2_ CH4						UART 1_RTS	UART 2_RX/ UART 2_TX	UART 3_RTS	UART 4_RX/ UART 4_TX	UART 5_RTS	UART6 _RX/U ART6_ TX	TIM1 _CH1	CAN _TX
PA4/A IN4	SPI1_ NSS				TIM14 _CH1				UART 1_TX/ UART 1_RX	UART 2_CTS	UART 3_TX/ UART 3_RX	UART 4_CTS	UART 5_TX/ UART 5_RX	UART6 _CTS	TIM1 _CH1 N	CAN _RX
PA5/A IN5	SPI1_ SCK	TIM2_ ETR	TIM2_ CH1						UART 1_RX/ UART 1_TX	UART 2_RTS	UART 3_RX/ UART 3_TX	UART 4_RTS	UART 5_RX/ UART 5_TX	UART6 _RTS	TIM1 _CH2	CAN _TX
PA6/A IN6	SPI1_ MISO	TIM3_ CH1	TIM2_ CH2			TIM16 _CH1	CM0_ TXEV	COMP 1_OU T	UART 1_CTS	UART 2_TX/ UART 2_RX	UART 3_CTS	UART 4_TX/ UART 4_RX	UART 5_CTS	UART6 _TX/U ART6_ RX	TIM1 _CH2 N	CAN _RX
PA7/A IN7	SPI1_ MOSI	TIM3_ CH2	RCC_ MCO	TIM2_ CH3	TIM14 _CH1		CM0_ TXEV		UART 1_RTS	UART 2_RX/ UART 2_TX	UART 3_RTS	UART 4_RX/ UART 4_TX	UART 5_RTS	UART6 _RX/U ART6_ TX	TIM1 _CH3	CAN _TX
PA8	RCC_ MCO			CM0_ TXEV					UART 1_TX/ UART 1_RX	UART 2_CTS	UART 3_TX/ UART 3_RX	UART 4_CTS	UART 5_TX/ UART 5_RX	UART6 _CTS	TIM1 _CH1	CAN _RX
PA9	TIM1 5_BKI N	TIM2_ ETR	TIM2_ CH1		I2C1_ SCL	RCC_ MCO			UART 1_RX/ UART 1_TX	UART 2_RTS	UART 3_RX/ UART 3_TX	UART 4_RTS	UART 5_RX/ UART 5_TX	UART6 _RTS	TIM1 _CH1 N	CAN _TX
PA10			EXT_T RIG	TIM2_ CH2	I2C1_ SDA	Trace_ TX			UART 1_CTS	UART 2_TX/ UART 2_RX	UART 3_CTS	UART 4_TX/ UART 4_RX	UART 5_CTS	UART6 _TX/U ART6_ RX	TIM1 _CH2	CAN _RX
PA11	CM0_ TXEV	UART 1_CTS	TIM2_ CH3						UART 1_RTS	UART 2_RX/ UART 2_TX	UART 3_RTS	UART 4_RX/ UART 4_TX	UART 5_RTS	UART6 _RX/U ART6_ TX	TIM1 _CH2 N	CAN _TX
PA12	CM0_ TXEV	UART 1_RTS	TIM2_ CH4						UART 1_TX/ UART 1_RX	UART 2_CTS	UART 3_TX/ UART 3_RX	UART 4_CTS	UART 5_TX/ UART 5_RX	UART6 _CTS	TIM1 _CH3	CAN _RX
PA13_ SWDI O	CM0_ SWD	IRTIM _IROU T	EXT_T RIG						UART 1_RX/ UART 1_TX	UART 2_RTS	UART 3_RX/ UART 3_TX	UART 4_RTS	UART 5_RX/ UART 5_TX	UART6 _RTS	TIM1 _CH3 N	
PA14_ SWCL	CM0_ SWCL					Trace_ TX	TIM1_ ETR		UART 1_TX/ UART	UART 2_CTS	UART 3_TX/ UART	UART 4_CTS	UART 5_TX/ UART	UART6 _CTS	TIM1 _CH4	

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
K	K								1_RX		3_RX		5_RX			
PA15	SPI1_NSS	TIM2_ETR	TIM2_CH1	CM0_TXEV	EXT_TRIG	Trace_TX			UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH3N	CAN_TX
PB0/AIN8	CM0_TXEV	TIM3_CH3	TIM2_CH4						UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH3N	
PB1/AIN9	TIM14_CH1	TIM3_CH4				Trace_TX	COMP2_OUT	COMP3_OUT	UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH1	
PB2/AIN10		TIM2_ETR	TIM2_CH1	I2C1_SMBA					UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH1N	
PB3	SPI1_SCK	CM0_TXEV	TIM2_CH2						UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH1	CAN_RX
PB4	SPI1_MISO	TIM3_CH1	CM0_TXEV	TIM2_CH3	TIM3_ETR				UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH1N	CAN_TX
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	TIM2_CH4				UART1_TX/UART1_RX	UART2_RX/UART2_TX	UART3_TX/UART3_RX	UART4_RX/UART4_TX	UART5_TX/UART5_RX	UART6_RX/UART6_TX	TIM1_CH2	CAN_RX
PB6		I2C1_SCL	TIM16_CH1N						UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH2N	CAN_TX
PB7		I2C1_SDA	TIM2_CH2		EXT_TRIG			COMP3_OUT	UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH3	CAN_RX
PB8		I2C1_SCL	TIM16_CH1						UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH3	CAN_RX
PB9	IRTIM_IROUT	I2C1_SDA		CM0_TXEV					UART1_RX/UART1_TX	UART2_TX/UART2_RX	UART3_RX/UART3_TX	UART4_TX/UART4_RX	UART5_RX/UART5_TX	UART6_TX/UART6_RX	TIM1_CH3N	CAN_TX
PB10/AIN11		I2C1_SCL	TIM2_CH2						UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH2	CAN_RX
PB11/AIN12	CM0_TXEV	I2C1_SDA	TIM2_CH3						UART1_RX/UART1_TX	UART2_RX/UART2_TX	UART3_RX/UART3_TX	UART4_RX/UART4_TX	UART5_RX/UART5_TX	UART6_RX/UART6_TX	TIM1_CH2N	CAN_TX
PB12/AIN13	SPI1_NSS	CM0_TXEV	TIM2_CH1	TIM2_ETR		TIM15_BKIN		COMP1_OUT	UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH3	CAN_RX
PB13/AIN14	SPI1_SCK		TIM2_CH2					COMP2_OUT	UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH3N	CAN_TX
PB14/	SPI1_	TIM15	TIM2_				TIM1_	COMP3_OUT	UART	UART2_TX/	UART	UART4_TX/	UART	UART6_TX/U	TIM1	

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
AIN15	MISO	_CH1	CH3				ETR	T	1_CTS	UART2_RX	3_CTS	UART4_RX	5_CTS	ART6_RX	_CH4	
PB15	SPI1_MOSI	TIM15_CH2	TIM2_CH4	TIM15_CH1N					UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_BKIN	
PC12							TIM1_ETR		UART1_TX/UART1_RX	UART2_TX/UART2_RX	UART3_TX/UART3_RX	UART4_TX/UART4_RX	UART5_TX/UART5_RX	UART6_TX/UART6_RX	TIM1_CH4	
PC13									UART1_RX/UART1_TX	UART2_RX/UART2_TX	UART3_RX/UART3_TX	UART4_RX/UART4_TX	UART5_RX/UART5_TX	UART6_RX/UART6_TX	TIM1_BKIN	
PC14_OSC32_IN		TIM2_ETR	TIM2_CH1						UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH1	
PC15_OSC32_OUT			TIM2_CH4			Trace_TX			UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH1N	
PF0_OSC_IN		I2C1_SDA	TIM2_CH1	TIM2_ETR					UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH2	
PF1_OSC_OUT		I2C1_SCL	TIM2_CH2			Trace_TX			UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH2N	
PF6		I2C1_SCL					TIM1_ETR		UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH4	
PF7		I2C1_SDA			EXT_TRIG				UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_BKIN	
BOOT_PF8			TIM2_CH3	TIM3_CH3		Trace_TX			UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH3N	
NRST_PF9			TIM2_CH3						UART1_TX/UART1_RX	UART2_TX/UART2_RX	UART3_TX/UART3_RX	UART4_TX/UART4_RX	UART5_TX/UART5_RX	UART6_TX/UART6_RX	TIM1_BKIN	

## 7 Package characteristics

### 7.1 LQFP48

LQFP48 is a 7 x 7 mm, and 0.5 mm pitch package.

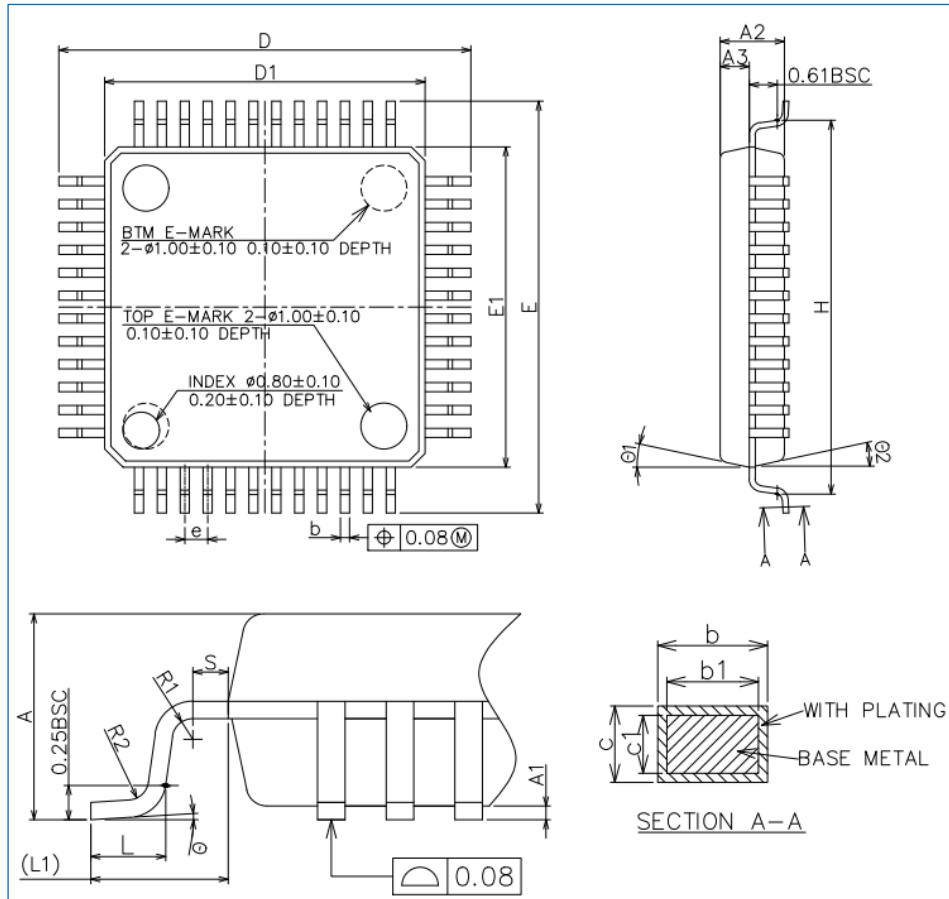


Figure 7-1 LQFP48 package outline

Table 7-1 LQFP48 package parameters

Symbol	Unit: mm			Unit: inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.18	-	0.27	0.0071	-	0.0106
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
e	0.40	0.50	0.60	0.0157	0.0197	0.0236
H	8.14	8.17	8.20	0.3205	0.3217	0.3228

Symbol	Unit: mm			Unit: inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
L	0.50	-	0.70	0.0197	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.2	-	-	0.0079	-	-
$\theta$	0°	3.5°	7°	-	-	-
$\theta_1$	11°	12°	13°	-	-	-
$\theta_2$	11°	12°	13°	-	-	-

## 7.2 LQFP44

LQFP44 is a 10mm x10mm, and 0.8 mm pitch package.

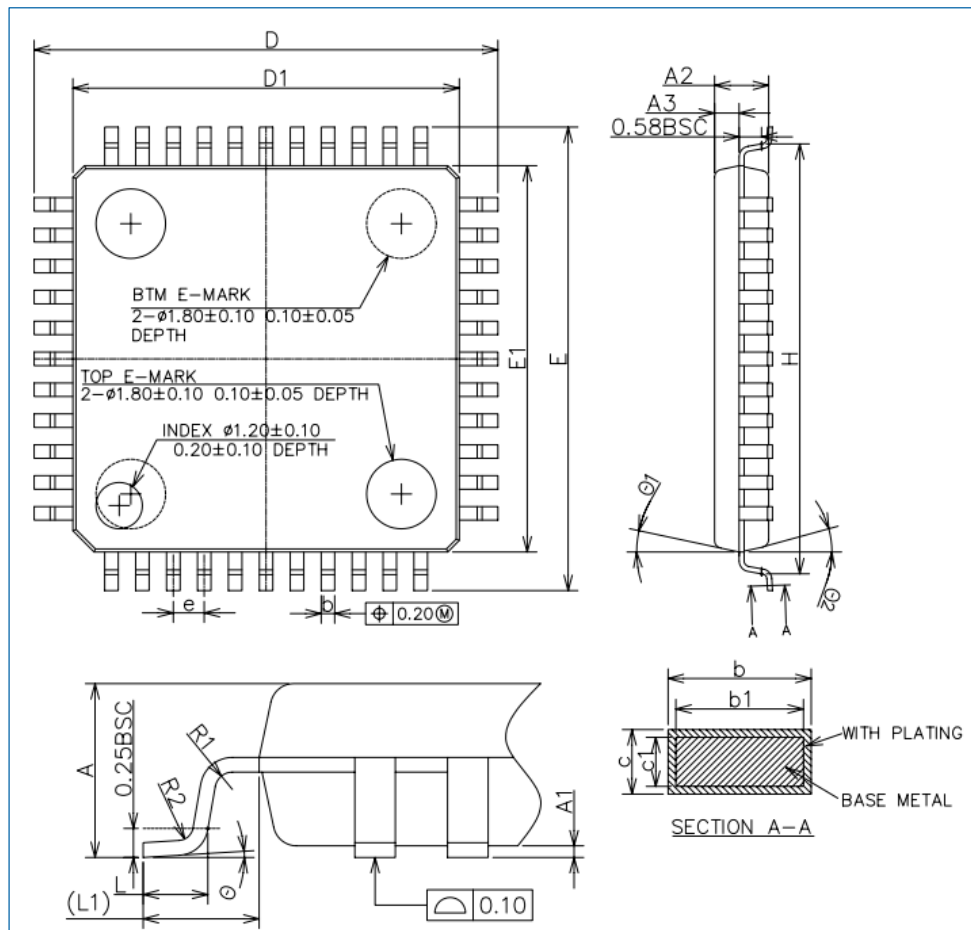


Figure 7-2 LQFP44 package outline

Table 7-2 LQFP44 package parameters

Symbol	millimeters			Inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.33	-	0.42	0.0130	-	0.0165

Symbol	millimeters			Inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	11.95	12.00	12.05	0.4705	0.4724	0.4744
D1	9.9	10.00	10.10	0.3898	0.3937	0.3976
E	11.95	12.00	12.05	0.4705	0.4724	0.4744
E1	9.90	10.00	10.10	0.3898	0.3937	0.3976
e	0.70	0.80	0.90	0.0276	0.0315	0.0354
H	11.09	11.13	11.17	0.4366	0.4382	0.4398
L	0.53	-	0.70	0.0209	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	-	0.15	-	-	0.0059	-
R2	-	0.13	-	-	0.0051	-
$\theta$	0°	3.5°	7°	0.0079	-	-
$\theta_1$	11°	12°	13°	-	-	-
$\theta_2$	11°	12°	13°	-	-	-

### 7.3 LQFP32

LQFP32 is a 7 mm x 7 mm and 0.8 mm pitch package.

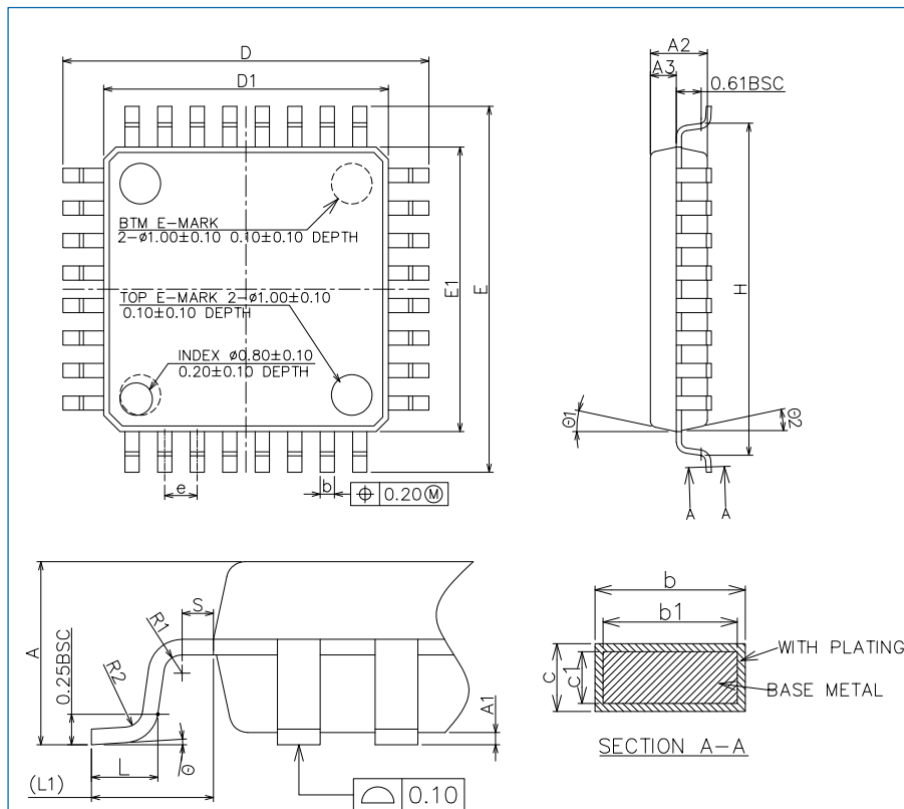


Figure 7-3 LQFP32 package outline

Table 7-3 LQFP32 package parameters

Symbol	millimeters			Inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.33	-	0.42	0.0130	-	0.0165
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
e	0.70	0.80	0.90	0.0276	0.0315	0.0354
H	8.14	8.17	8.20	0.3205	0.3217	0.3228
L	0.50	-	0.70	0.0197	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
θ	0°	3.5°	7°	-	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

## 7.4 TSSOP24

TSSOP24 is a 7.8 mm x 4.4 mm and 0.65 mm pitch package.

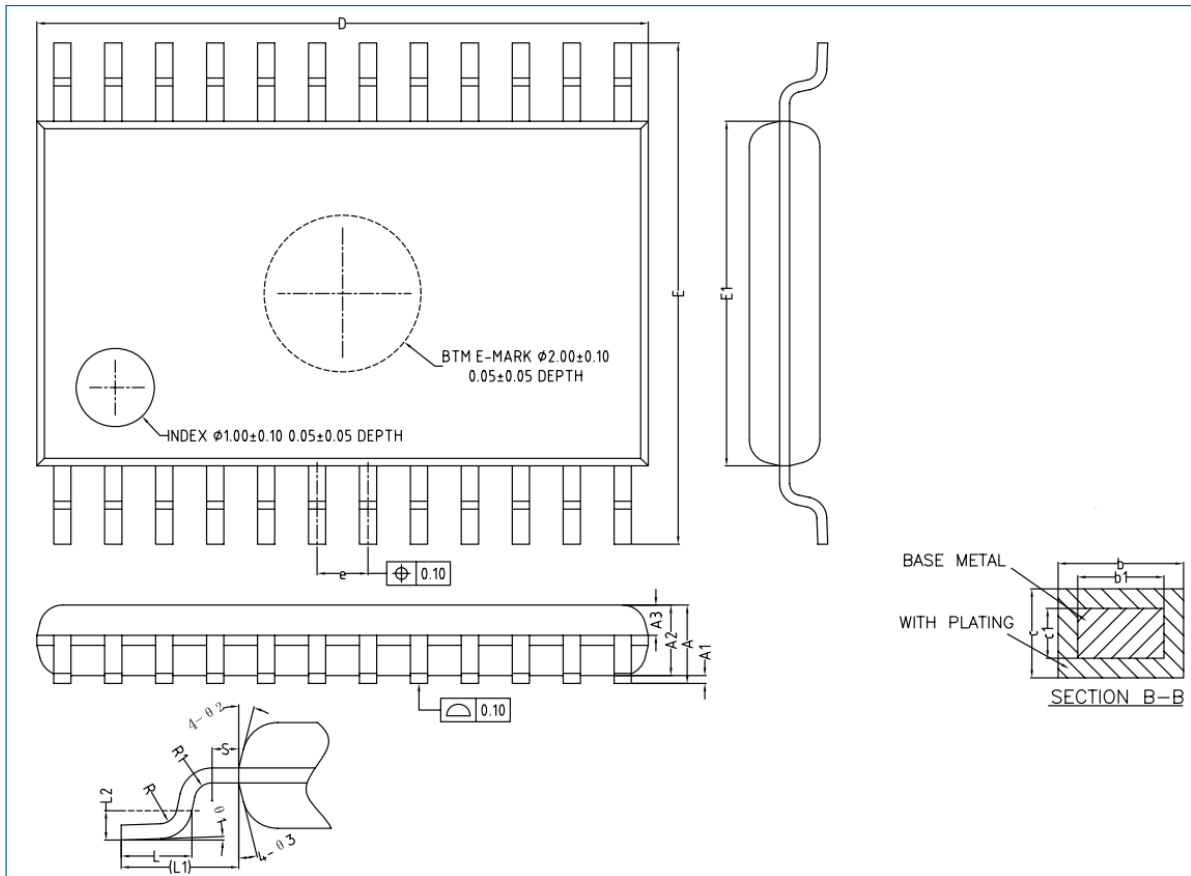


Figure 7-4 TSSOP24 package outline

Table 7-4 TSSOP24 package parameters

Symbol	millimeters			Inches <sup>(1)</sup>			
	Min	Typ	Max	Min	Typ	Max	Max
A	-	-	1.20	-	-	0.0472	
A1	0.05	-	0.15	0.0020	-	0.0059	
A2	0.80	0.90	1.00	0.0315	0.0354	0.0394	
b	0.20	-	0.29	0.0079	-	0.0114	
b1	0.19	0.22	0.25	0.0075	0.0087	0.0098	
c	0.10	-	0.19	0.0039	-	0.0075	
c1	0.10	0.13	0.15	0.0039	0.0051	0.0059	
D	7.70	7.80	7.90	0.3031	0.3071	0.3110	
E	6.20	6.40	6.60	0.2441	0.2520	0.2598	
E1	4.30	4.40	4.50	0.1693	0.1732	0.1772	
e	0.55	0.65	0.75	0.0217	0.0256	0.0295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295	
L1	-	1.00	-	-	0.0394	-	
L2		0.25		0.0000	0.0098	0.0000	
R	0.09	-	-	0.0035	-	-	
R1	0.09	-	-	0.0035	-	-	
S	0.20	-	-	0.0079	-	-	
$\theta$	0°	-	8°	-	-	-	
$\theta 1$	12°	14°	16°	-	-	-	

Symbol	millimeters			Inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
θ2	12°	14°	16°	-	-	-
θ3	12°	14°	16°	-	-	-

## 8 Ordering information

Table 8-1 HK32APIN02x ordering information

Package	HK32APIN02x series	Package	Comments
LQFP48	HK32ASPIN021C8T7	Tape and reel /Tray	The pinouts in two modes are minorly different, check Figure 6-1 for details.
	HK32ASPIN022C8T7	Tape and reel /Tray	
LQFP44	HK32ASPIN020S8T7	Tape and reel /Tray	-
LQFP32	HK32ASPIN020K8T7	Tape and reel /Tray	The pinouts in three modes are minorly different, check Figure 6-3 for details.
	HK32ASPIN021K8T7	Tape and reel /Tray	
	HK32ASPIN022K8T7	Tape and reel /Tray	
TSSOP24	HK32ASPIN020E8P7	Tape and reel/Tube	-

## 9 Glossary and Abbreviations

Name	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-Wakeup
CRC	Cyclic Redundancy Check
CSS	Clock Security System
DMA	Direct Memory Access
EXTI	Extended Interrupts and Events Controller
FSMC	Flexible Static Memory Controller
GPIO	General Purpose Input Output
HSE	High Speed External (Clock Signal)
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-Speed Internal (Clock Signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-Down Reset
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous Asynchronous Receiver Transmitter
WWDG	Window Watchdog

## 10 Legal and Contact Information



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