HK32F103x8xBT6A Datasheet

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Preface

Purpose

This document introduces the block diagram, the memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F103x8xBT6A Series SOC, to help users quickly understand its features and functions.

Audience

This document is intended for:

- HK32F103 x8xBT6A Developer
- HK32F103 x8xBT6A Tester
- HK32F103 x8xBT6A user

Release Notes

This document is corresponding to HK32F103x8xBT6A Series SOC.

Revision History

Version	Date	Description
1.0.0	2018/06/08	Initial Release
1.1.0	2019/10/22	Add *Section 3.27 DVSQ unit*.
1.1.1	2020/06/19	Update *Section 3.14 DMA.*
1.1.2	2020/08/23	Update *Section 3.9.1 Clock tree.*
1.1.3	2021/01/26	Update *Section 4.2.14 ADC characteristics.*
1.1.4	2021/07/06	Update *Section 3.2 Memory mapping*.
1.1.5	2021/08/11	Add *Section 3.9 Reset*
1.2	2022/10/24	Deleted *Section 3.5 Coprocessor, and all related description.*

Contents

1 Introduction

This document is the datasheet for HK32F103x8xBT6A series System-on-Chips (SOCs). HK32F103x8xBT6A is a family of low-power microcontrollers (MCU) developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd, including:

- HK32F103x8T6A
  - HK32F103C8T6A
  - HK32F103R8T6A
  - HK32F103V8T6A
- HK32F103xBT6A
  - HK32F103CBT6A
  - HK32F103RBT6A
  - HK32F103VBT6A

Please refer to HK32F103x8xBT6A Reference Manual for more details.

2 HK32F103x8xBT6A Overview

Based on ARM® Cortex®-M3 core, HK32F103x8xBT6A embeds medium capacity memories, including a 64-/128-Kbyte Flash, a 20-Kbyte SRAM. Its maximum frequency is 120 MHz.

HK32F103x8xBT6A embeds an advanced timer and three general-purpose timers.

HK32F103x8xBT6A integrates communication interfaces: two SPIs, two I2Cs, three USARTs, a full speed USB2.0 interface, a CAN, two 12-bit SAR ADCs, and an on-chip temperature sensor.

With its various peripheral interfaces, HK32F103x8xBT6A is suitable for a wide range of applications:

- Industry application, such as programmable controllers, printers, and scanners
- Motor drive and speed control
- Low-power terminals with sensors for Internet of Things
- UAV flight control, pylon control
- Toy products
- Household appliances
- Intelligent robots
- Smart watches and sports bracelets

2.1 Features

- CPU core
  - ARM® Cortex®-M3 core
  - Maximum frequency: 120 MHz
  - 24-bit SysTick timer
  - Supports output the Event signal to MCU pins (to co-work with others system-on-chip CPUs)
- Operating voltage range
  - Main power supply (V_{DD}):2.0 V to 3.6 V
  - Back-up power supply (V_{BAT}): 1.8 V to 3.6 V
  - When the main power is powered down, the RTC continues to operate with V_{BAT} supply.
  - When the main power is powered down, 20-byte backup registers are available with V_{BAT} supply.
- Operating temperature range: -40°C to +105°C
- Typical operating current (V_{DD})
  - Run mode: 20.95mA@120MHz@3.3V
  - Sleep mode: 14.63 mA@120MHz@3.3V
  - Stop mode:
    - LDO Full-speed running: 303μA@3.3V
    - LDO low-power mode: 89.67μA@3.3V
  - Standby mode: 3.36μA@3.3V
- Memory
  - 64- or 128- Kbyte Flash
    - When the CPU frequency is not more than 26.5 MHz, MCU supports zero wait state
    - Flash data security protection function (read or write protection can be set respectively)
  - 20-Kbyte SRAM
- DMA controller

- 7 channels
- Supports triggering by peripherals, such as timer, ADC, SPI, I2C and USART

- Clock
  - External high-speed clock (HSE): 4-32 MHz (typical value: 8 MHz)
  - External low-speed clock (LSE): 32.768 kHz
  - Internal high-speed clock (HSI): 56MHz/28 MHz/8 MHz
  - Internal low-speed clock (LSI): 40 kHz
  - PLL clock
- Reset
  - External pin reset
  - POR/PDR reset
  - Software reset
  - Watchdog timer reset (IWDG and WWDG)
  - Low-power mode reset
- GPIO
  - Up to 80 GPIOs for 100-pin package/ 51 GPIOs for 64-pin package / 37 GPIOs for 48-pin package
  - Each GPIO can be configured as an external interrupt input
  - Provides up to 20 mA driving current
- Data security
  - CRC verification hardware unit
- Data communication interfaces
  - 3 x USARTs (supports ISO-7816 smart card protocol)
  - 2 x SPIs (supports the I2S protocol)
  - 2 x I2Cs
  - 1 x CAN 2.0A/2.0B
  - 1 x Full Speed (FS) USB2.0
- Timer
  - 1 x Advanced Timer: TIM1 (Channel 1-3 support output with programmable inserted dead-times and the break function)
  - 3 x general-purpose timers: TIM2/TIM3/TIM4
- RTC clock counter cooperates with the software to provide a clock-calendar function.
- Programmable voltage detection (PVD)
  - Configurable 8 levels detecting voltage thresholds
  - Configurable rising edge or falling edge for detecting
- On-chip analog circuity
  - 2 x 12-bit successive approximation register (SAR) ADCs
    - 10/16 analog input channels
    - Up to 1MSPS conversion frequency
    - Supports automatic scan and scan conversion
    - When cascaded, it supports master-slave parallel conversion and interleaved conversion
  - 1 x temperature sensor
    - The analog output connects to an ADC channel

- CPU Trace and debug
  - SW-DP 2-wire debug port
  - JTAG 5-wire debug port
  - ARM trace and debug modules, such as data watchpoint and trace (DWT), Flash address reload and breakpoint (FPB), Instrumentation Trace Macrocell (ITM), trace port interface unit (TPIU)
- Reliability
  - Passed HBM2000V/CDM500V/MM200V/LU level tests

2.2 Device overview

Table 2-1 HK32F103x8xBT6A series features

Features		HK32F103CxT6A		HK32F103RxT6A		HK32F103VxT6A	
		HK32F103C8T6A	HK32F103CBT6A	HK32F103R8T6A	HK32F103RBT6A	HK32F103V8T6A	HK32F103VBT6A
Operating voltage		● V_{DD}：2.0~3.6V ● V_{BAT}：1.8~3.6V					
Operating temperatures		-40 - +105 °C					
CPU	Core	Cortex®-M3					
	Frequency	120 MHz					
Flash (Kbyte)		64	128	64	128	64	128
SRAM (Kbyte)		20		20		20	
Clock		LSI：30~60 kHz, typical frequency 40 kHz HSI：56MHz/28 MHz/8 MHz LSE：32.768 kHz HSE：4~32 MHz PLLCLK：supported GPIO Clock：up to 64 MHz					
Timers	General-purpose	TIM2/3/4					
	Advanced-control	TIM1					
Peripherals	SPI	2					
	I2C	2					
	USART	3					
	USB	1					
	CAN	1					
ADC		2（10 channels）		2（16 channels）		2（16 channels）	
GPIO		37		51		80	
Packages		LQFP48		LQFP64		LQFP100	

3 Function Description

3.1 Block diagram

ARM® Cortex®-M3 is a 32-bit RISC processor, which provides a MCU platform with low-cost, high-performance and low-power consumption features. It delivers outstanding computational performance and an advanced system response to interrupts. With its embedded ARM Cortex-M3 core, HK32F103x8xBT6A family is compatible with ARM tools and software.

The block diagram of HK32F103x8xBT6A shows as follows:

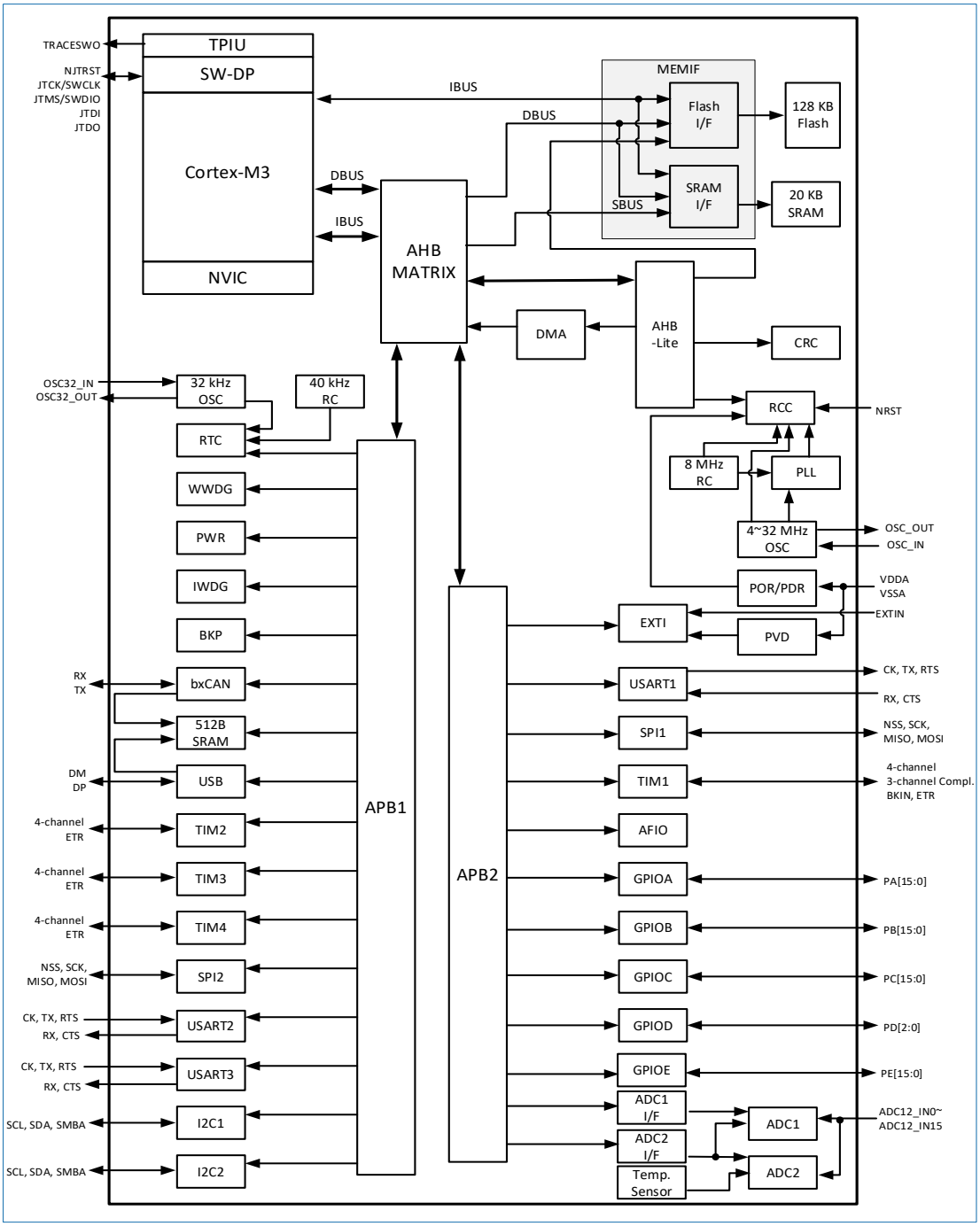

Figure 3-1 HK32F103x8xBT6A block diagram

3.2 Memory mapping

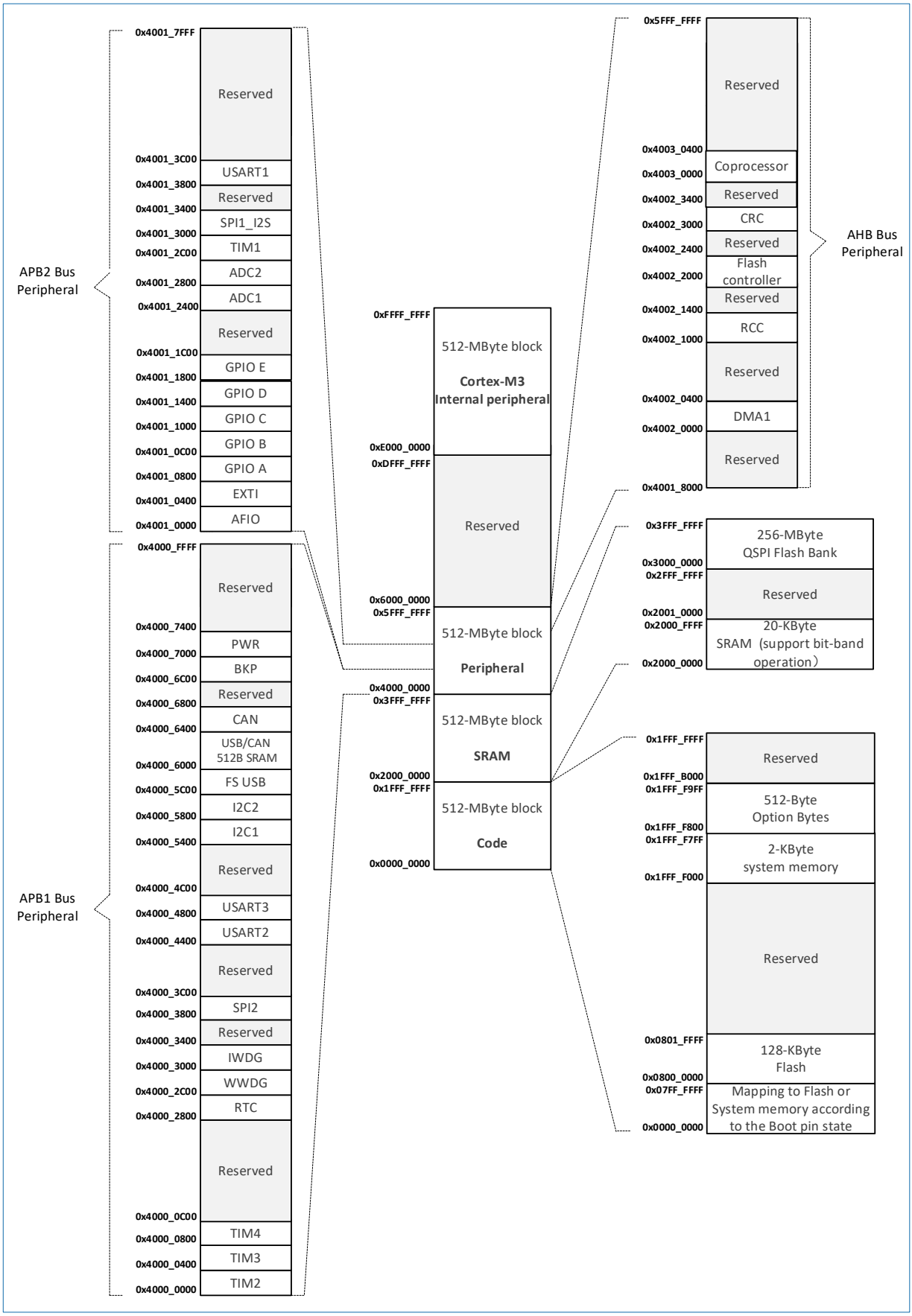

Figure 3-2 Memory mapping

3.3 Flash

HK32F103x8xBT6A integrates a 64 or 128 Kbytes Flash memory to store programs and data. The Flash supports one hundred thousand cycles erase.

3.4 SRAM

HK32F103x8xBT6A integrates a 20 Kbytes SRAM. CPU can access SRAM fast with zero wait state to meet the requirements of most applications.

3.5 CRC

CRC is used to verify data transmission or storage integrity. HK32F103x8xBT6A integrates a CRC calculation unit to reduce user application processing burden and to provide process-accelerating capability.

CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 NVIC

HK32F103x8xBT6A embeds a nested vectored interrupt controller (NVIC) to handle interrupt flexibly with low interrupt latency. NVIC can handle up to 50 maskable interrupt channels (excluding Cortex-M3 interrupt lines) and 16 level priorities.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Supports tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

Table 3-1 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0X0000_0000
-	-3	Fixed	Reset	Reset	0X0000_0004
-	-2	Fixed	NMI	Non-maskable interrupt The RCC Clock Security System (CSS) is linked to the NMI vector.	0X0000_0008
-	-1	Fixed	HardFault	All class of fault	0X0000_000C
-	0	Settable	MemManage	Memory management	0X0000_0010
-	1	Settable	BusFault	Pre-fetch fault, memory access fault	0X0000_0014
-	2	Settable	UsageFault	Undefined instruction or illegal state	0X0000_0018
-	-	-	-	Reserved	0X0000_001C - 0X0000_002B
-	3	Settable	SVCall	System service call via SWI instruction	0X0000_002C
-	4	Settable	DebugMonitor	Debug Monitor	0X0000_0030
-	-	-	-	Reserved	0X0000_0034
-	5	Settable	PendSV	Pendable request for system service	0X0000_0038
-	6	Settable	SysTick	System tick timer	0X0000_003C

Position	Priority		Name	Description	Address
0	7	Settable	WWDG	Window watchdog interrupt	0X0000_0040
1	8	Settable	PVD	PVD through EXTI Line detection interrupt	0X0000_0044
2	9	Settable	TAMPER	Tamper interrupt	0X0000_0048
3	10	Settable	RTC	RTC global interrupt	0X0000_004C
4	11	Settable	FLASH	Flash global interrupt	0X0000_0050
5	12	Settable	RCC	RCC global interrupt	0X0000_0054
6	13	Settable	EXTI0	EXTI Line0 interrupt	0X0000_0058
7	14	Settable	EXTI1	EXTI Line1 interrupt	0X0000_005C
8	15	Settable	EXTI2	EXTI Line2 interrupt	0X0000_0060
9	16	Settable	EXTI3	EXTI Line3 interrupt	0X0000_0064
10	17	Settable	EXTI4	EXTI Line4 interrupt	0X0000_0068
11	18	Settable	DMA_Channel1	DMA Channel1 global interrupt	0X0000_006C
12	19	Settable	DMA_Channel2	DMA Channel2 global interrupt	0X0000_0070
13	20	Settable	DMA_Channel3	DMA Channel3 global interrupt	0X0000_0074
14	21	Settable	DMA_Channel4	DMA Channel4 global interrupt	0X0000_0078
15	22	Settable	DMA_Channel5	DMA Channel5 global interrupt	0X0000_007C
16	23	Settable	DMA_Channel6	DMA Channel6 global interrupt	0X0000_0080
17	24	Settable	DMA_Channel7	DMA Channel7 global interrupt	0X0000_0084
18	25	Settable	ADC1_2	ADC1 and ADC2 global interrupt	0X0000_0088
19	26	Settable	USB_HP_CAN_TX	USB high priority or CAN TX interrupts	0X0000_008C
20	27	Settable	USB_LP_CAN_RX0	USB low priority or CAN RX0 interrupts	0X0000_0090
21	28	Settable	CAN_RX1	CAN RX1 interrupt	0X0000_0094
22	29	Settable	CAN_SCE	CAN SCE interrupt	0X0000_0098
23	30	Settable	EXTI9_5	EXTI Line[9:5] interrupts	0X0000_009C
24	31	Settable	TIM1_BRK	TIM1 Break interrupt	0X0000_00A0
25	32	Settable	TIM1_UP	TIM1 Update interrupt	0X0000_00A4
26	33	Settable	TIM1_TRG_COM	TIM1 Trigger and Commutation interrupts	0X0000_00A8
27	34	Settable	TIM1_CC	TIM1 Capture Compare interrupt	0X0000_00AC
28	35	Settable	TIM2	TIM2 global interrupt	0X0000_00B0
29	36	Settable	TIM3	TIM3 global interrupt	0X0000_00B4
30	37	Settable	TIM4	TIM4 global interrupt	0X0000_00B8
31	38	Settable	I2C1_EV	I2C1 event interrupt	0X0000_00BC
32	39	Settable	I2C1_ER	I2C1 error interrupt	0X0000_00C0
33	40	Settable	I2C2_EV	I2C2 event interrupt	0X0000_00C4
34	41	Settable	I2C2_ER	I2C2 error interrupt	0X0000_00C8
35	42	Settable	SPI1	SPI1 global interrupt	0X0000_00CC
36	43	Settable	SPI2	SPI2 global interrupt	0X0000_00D0
37	44	Settable	USART1	USART1 global interrupt	0X0000_00D4
38	45	Settable	USART2	USART2 global interrupt	0X0000_00D8
39	46	Settable	USART3	USART3 global interrupt	0X0000_00DC
40	47	Settable	EXTI15_10	EXTI Line[15:10] interrupts	0X0000_00E0

Position	Priority		Name	Description	Address
41	48	Settable	RTCAlarm	RTC alarm through EXTI line interrupt	0X0000_00E4
42	49	Settable	USBWakeUp	USB wakeup from suspend through EXTI line interrupt	0X0000_00E8
43	50	-	-	Reserved	0X0000_00EC
44	51	-	-	Reserved	0X0000_00F0
45	52	-	-	Reserved	0X0000_00F4
46	53	-	-	Reserved	0X0000_00F8
47	54	-	-	Reserved	0X0000_00FC
48	55	-	-	Reserved	0X0000_0100
49	56	-	-	Reserved	0X0000_0104

3.7 EXTI

The external interrupt/event (EXTI) controller contains 19 edge detectors, and generates interrupt/event request. The trigger event of each EXTI line can be configured and masked independently. HK32F103x8xBT6A has a pending register to maintain all interrupt request states.

3.8 Reset

HK32F103x8xBT6A supports System reset, Power reset and Backup domain reset.

3.8.1 System reset

Except for the reset flags in the RCC_CSR register and registers in the backup domains, System reset signal resets all the registers.

When one of the following events occurs, System Reset signal is generated:

- Low-level voltage on NRST pin (External Reset)
- Window watchdog counting terminates (WWDG Reset)
- Independent watchdog counting terminates (IWDG Reset)
- Software reset (SW Reset)
- Low-power consumption management reset

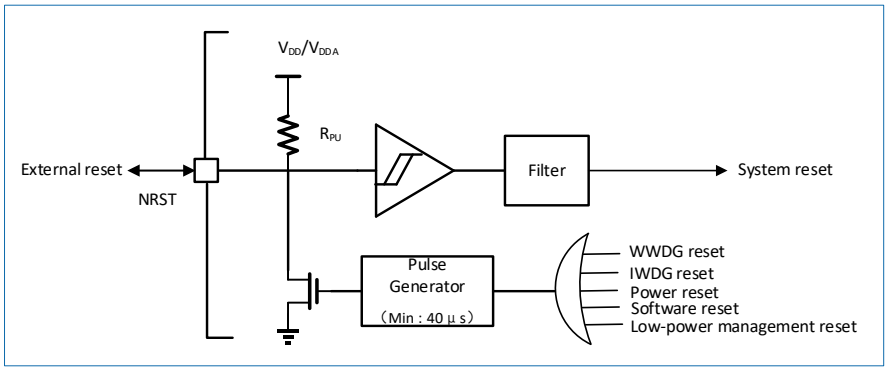

Figure 3-3 System reset

An Internal Reset signal is output via the NRST pin. A Pulse generator guarantees that each reset source produces at least 40 μs pulse latency. When NRST pin is pulled down, a reset pulse is generated for an external reset.

You can identify a reset source by checking reset state flags in the RCC_CSR register.

Table 3-2 Reset setting

Software reset	By setting the SYSRESETREQ bit to '1' or generating a Cortex-M3 interrupt to perform Software

	reset.
Low-power consumption management reset	To generate a low-power management reset signal when entering Standby mode: Set the nRST_STDBY bit in Option bytes to '0' to enable the low-power management reset function. Then, even it is in the process of entering Standby mode, the system will be reset instead of entering Standby mode.
	To generate a low-power management reset signal when entering Stop mode: Set the nRST_STOP bit in Option bytes to '0' to enable the low-power management reset function. Then, even it is in the process of entering Stop mode, the system will be reset instead of entering Stop mode.

3.8.2 Power reset

Power reset signal resets all registers except the registers in the backup domain. The reset source acts on the reset pin, and keeps low level in the progress of reset. Reset entry vector is fixed on address 0x0000_0004.

When the following event occurs, Power reset signal is generated:

- POR/PDR reset
- Return from Standby mode

HK32F103xCxDxE embeds POR/PDR circuitry. The circuitry always operates to ensure the system runs well with power supply over than POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, MCU resets and no external reset circuit is required.

3.8.3 Backup domain reset

Backup domain has two dedicated reset signals, which affect the backup domain only. When the following event occurs, backup domain reset signal is generated:

- Set BDRST bit in the RCC_BDCR register (trigger the software reset too).
- After both V_{DD} and V_{BAT} are powered down, power on V_{DD} or V_{BAT}.

3.9 Clock

HK32F103x8xBT6A selects a system clock when it starts. When it resets, 8 MHz HSI RC is selected by default as system clock. If it fails, an external clock with frequency in 4 to 32 MHz is selected as system clock. When the external clock fails, the system switches to select an internal RC oscillator. Meanwhile, if the software interrupt is enabled, an interrupt is generated as well.

Full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

3.9.1 Clock Source

Table 3-3 Clock source

Clock	Clock Source
HSI oscillator	Frequency: 56 MHz; which can be divided by 2 or 7. Accuracy: full temperature range ± 2%
HSE oscillator	4-32 MHz oscillator OSC_IN can be used as an external clock input (up to 64 MHz)
PLL clock	Input frequency: 2-56 MHz Output frequency: 30-120 MHz
LSI clock	Frequency: 30-60 kHz (typical: 40 kHz)
LSE clock	Frequency: 32.768 kHz OSC32_IN can be used as external clock input (32.768 kHz)
GPIO input clock	PA1, PB1, PC7, PB7 (up to 64 MHz)

3.9.2 Clock Tree

The clock tree shows as below:

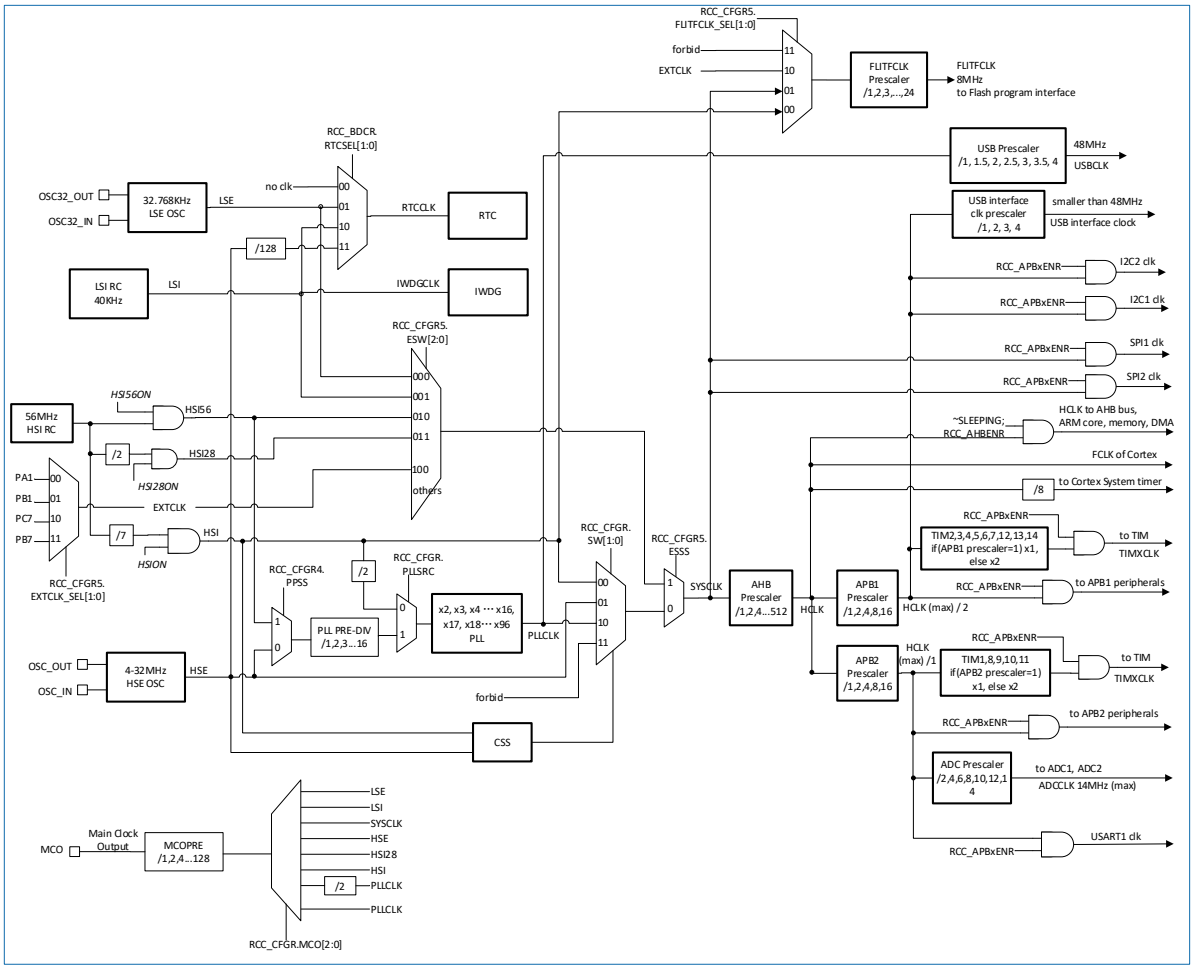

Figure 3-4 clock tree

PLL：chosen from HSI8M/2, HSI56M/PREDIV and HSE/PREDIV.

SYSCLK：chosen from HSI8M, HSI28M, HSI56M, HSE, PLL, LSI, LSE or GPIO input clock. HSI8M is the default clock.

FLITFCLK：chosen from HSI8M, GPIO input clock or SYSCLK clock.

3.10 Boot mode

The Boot pin is used to select one of the following modes when the system starts:

- Boot from Flash block
- Boot from the system memory
- Boot from the internal SRAM

Bootloader program is stored in the system memory and it can reprogram Flash via the USART interface.

3.11 Power Supply schemes

- V_{DD}: 2.0 V to 3.6 V

V_{DD} pin supplies power for I/O pins and internal LDOs.

- V_{DDA}: 2.0 V to 3.6 V

V_{DDA} pin supplies power for components in the analog domain, such as ADC and the temperature sensor.

- V_{BAT}: 1.8 V to 3.6 V

When V_{DD} is not present, V_{BAT} supplies power for RTC, the external 32 kHz oscillator and backup registers through power switch.

3.12 PVD

HK32F103x8xBT6A integrates a programmable voltage detector (PVD). The PVD monitors V_{DD} power supply and compare it with the V_{PVD} threshold. When V_{DD} is lower or higher than the V_{PVD} threshold, an interrupt is generated. The interrupt program sends an alarm warning or/and switches MCU into Safe mode. PVD is enabled by software.

3.13 Low-power modes

HK32F103x8xBT6A supports several low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources.

- Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

In Stop mode, MCU achieves the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all internal clocks, the PLL, the HSE oscillators and the HSI oscillators are disabled. MCU can be woken up from Stop mode by any EXTI line. The EXTI line source can be one of external I/O pins, a PVD output, a RTC alarm or a USB wakeup signal.

- Standby mode

In Standby mode, MCU achieves the lowest power consumption. The internal LDO is off. The PLL, the HSE oscillators and the HSI oscillators are disabled. In Standby mode, the content in SRAM and registers is lost except for the one of registers in the backup domain, and the Standby circuitry is still working.

MCU exits from Standby mode when an external reset (NRST), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

For more information of power consumption in different modes, please see Table 4-6.

3.14 DMA

The flexible general-purpose DMA (7 channels for DMA) manages the transfers from memories to memories, devices to memories, and memories to devices. The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Every channel has a dedicated hardware DMA request logic and can be triggered by software. Transfer sizes, source address and destination address can be set independently by software. DMA can serve for the main peripherals, such as SPI, I2C, USART, timers, SDIO and ADC.

3.15 RTC and BKP

Real Time Clock (RTC) and the backup registers use a switch to control power supply. When V_{DD} is present, it is switched to V_{DD} to supply power, otherwise it is switched to the V_{BAT} pin.

3.15.1 RTC

RTC provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt.

The driven clock of RTC might be a 32.768 kHz external oscillator or an internal low-power RC oscillator. The typical frequency of the internal RC oscillator is 40 kHz. The RTC can be calibrated by using an external 512 Hz output to compensate for any natural quartz deviation. The RTC has a 32-bit programmable counter for long term measurement by together using the Compare register to generate an alarm. A 20-bit pre-scaler is used for the time clock and is by default configured to generate a time base of one second from the clock at 32.768 kHz.

3.15.2 BKP

Backup registers (BKP) are used to store user application data. The system reset and power reset signals do not reset these registers. When MCU is woken up from Standby mode, the registers are not reset neither.

3.16 Independent Watchdog

Independent watchdog (IWDG) is clocked from an internal independent 40 kHz RC. The IWDG is based on a 12-bit down counter and an 8-bit pre-scaler. Because it is independent from the main clock, IWDG can operate in Stop mode and Standby mode. It can be used as a watchdog to reset the system when a problem occurs or as a free running timer for application timeout management. IWDG can be configured to a software or hardware watchdog through Option bytes. In debug mode, the counter can be frozen.

3.17 Window Watchdog

Window watchdog (WWDG) is based on a 7-bit down counter. The counter can be set to the free running mode or used as a watchdog to reset the system when a problem occurs. It is clocked from the system clock and has an early warning interrupt capability. In debug mode, the counter can be frozen.

3.18 SysTick Timer

SysTick timer is dedicated to the operation system as a standard down counter. It features:

- 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.19 General-purpose Timer

Every general-purpose timer (TIM2/TIM3/TIM4) provides a 16-bit auto-reload up/down counter, a 16-bit programmable pre-scaler and 4 independent channels. Every channel can be used for input capture, output compare, PWM and single-pulse output.

General-purpose timers can corporate with advanced timers through Timer Linking feature for synchronization and event chaining. In debug mode, the counter can be frozen. Any of the general-purpose timers can be used to generate PWM outputs. Every general-purpose timer supports an independent DMA request mechanism.

3.20 Advanced Timer

HK32F103x8xBT6A integrates an advanced timer (TIM1).

The advanced timer can be regarded as a three-phase PWM generator on 6 channels, and used as a complete general-purpose timer. The 4 independent channels can used for:

- Input capture
- Output comparator
- PWM generation (edge or center-aligned modes)
- One-pulse mode output
- Complementary PWM outputs with programmable inserted dead-times

If configured as a standard 16-bit timer, an advanced timer has the same functions as the general-purpose timer. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%). Because most of its internal structure is the same as that of a general-purpose timer. The advanced timer can work together with general-purpose timers via Timer Link feature for synchronization or event chaining. In debug mode, the counter can be frozen.

3.21 I2C bus

HK32F103x8xBT6A integrates two I2C bus interfaces, which can work as a master or a slave and support standard or fast mode. The I2C interfaces support 7-bit or 10-bit addressing mode. They support double-slave address addressing in 7-bit slave mode. Each I2C interface embeds a hardware CRC generator/checker. They can be served by DMA and they support SMBus V2.0/PMBus.

3.22 USART

HK32F103x8xBT6A embeds three universal synchronous/asynchronous receiver transmitters (USART1/USART2/ USART3). These USART interfaces provide asynchronous communication, IrDA SIR ENDEC support, multi-proces sor communication, single-wire half-duplex communication and have LIN Master/Slave capability.

The USART1 is able to communicate at speeds up to 4.5Mbit/s. The other USART interfaces communicated at up to 2.25 Mbit/s.

All the USART interfaces provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant), and SPI-like communication capability.

3.23 SPI

HK32F103x8xBT6A has two SPI interfaces. In master or slave mode, full-duplex and half-duplex communicating speed is up to 18 Mbit/s. The 3-bit pre-scaler gives 8 master mode frequencies. Each frame can be configured to 8 or 16 bits. The hardware CRC generation/verification supports basic SD card and MMC modes.

All SPIs can be served by the DMA controller.

3.24 CAN

HK32F103x8xBT6A has an independent CAN interface. The CAN interface is compliant with Specification 2.0A and 2.0B (active). Its bit rate is up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifier as well as extended frames with 29-bit identifiers. It has 3 transmit mailboxes, 2 receive FIFOs, and 3 stages 14 scalable filter banks.

3.25 USB

HK32F103x8xBT6A embeds a USB interface, which is compatible with USB full-speed devices. It has software-configurable endpoint setting and suspend/resume function. The dedicated 48 MHz clock is generated by the internal PLL.

3.26 GPIO

Each of the GPIO pins can be configured by software as output (push- pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable. The I/Os alternate function configuration can be locked in order to avoid spurious writing to the I/O registers.

3.27 ADC

HK32F103x8xBT6A embeds two 12-bit ADCs. The two ADCs multiplex up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, the conversion on the specified group of analog input executes automatically.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single sample

The ADC can be served by DMA controller.

The analog watchdog feature allows to monitor the converted voltage of one channel, multiple channels, all selected channels. When the monitored voltage is lower or higher than the preset threshold, an interrupt is generated. The events generated by general-purpose timers and advanced timers can connect to the ADC start trigger and injection trigger respectively, to allow the application to synchronize A/D conversion and timers.

3.28 Temperature sensor

Temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel, which is used to convert the sensor output voltage into a digital value.

3.29 Debug Interface

Build-in ARM SWJ-DP interface, which is combined with a single wire debug interface, to perform the connection between serial single wire debug interfaces (SWDIO and SWCLK). The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

4 Electrical characteristics

4.1 Absolute maximum values

Note：

- *Stresses above the absolute maximum rating listed in Table 4-1 and Table 4-18 may cause permanent damage to the device.*
- *Exposure to maximum permitted conditions for extended periods may affect device reliability.*

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.5	6.0	V
V_{IN}	Input voltage on pins	V_{SS} - 0.3	V_{DD} + 4.0	
$\|\Delta V_{DDx}\|$	Variation between different V_{DD} Power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variation between different V_{DD} ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) (1)	150	mA
I_{VSS}	Total current out of Vss ground lines (sink) (1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$I_{INJ(PIN)}$ (2)	Injected current on pins (3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pin) (4)	±25	

(1). All main power (V_{DD}, V_{DDA}) and Ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

(2). Negative injected current disturbs the analog performance of the device.

(3). When $V_{IN} > V_{DD}$, a positive injected current is induced. When $V_{IN} < V_{SS}$, a negative injected current is induced, and the injected current must be limited to the permitted range.

(4). When several I/Os are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.1.3 Thermal characteristics

Table 4-3 Thermal characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-45 to +150	℃
T_J	Maximum junction temperature	125	

4.2 Operation conditions

4.2.1 General operation conditions

Table 4-4 General operation conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	60	
f_{PCLK2}	Internal APB2 clock frequency	0	120	
V_{DD}	Standard operating voltage	2	3.6	V
V_{DDA}	Analog operating voltage(1)	2	3.6	V
V_{BAT}	Backup operating voltage	1.8	3.6	V
T	operating temperature	-40	+105	℃

(1). All main power (V_{DD} and V_{DDA}) pins must always be connected to the external power supply.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0]=000	2.183	2.188	2.196	V
		PLS[2:0]=001	2.286	2.289	2.298	
		PLS[2:0]=010	2.393	2.399	2.407	
		PLS[2:0]=011	2.502	2.508	2.518	
		PLS[2:0]=100	2.621	2.629	2.639	
		PLS[2:0]=101	2.726	2.733	2.745	
		PLS[2:0]=110	2.839	2.846	2.855	
		PLS[2:0]=111	2.958	2.969	2.979	
	Programmable voltage detector level selection (falling edge)	PLS[2:0]=000	2.116	2.119	2.125	
		PLS[2:0]=001	2.208	2.211	2.220	
		PLS[2:0]=010	2.305	2.310	2.320	
		PLS[2:0]=011	2.399	2.406	2.416	
		PLS[2:0]=100	2.506	2.512	2.521	
		PLS[2:0]=101	2.596	2.602	2.613	
		PLS[2:0]=110	2.693	2.701	2.710	
		PLS[2:0]=111	2.798	2.805	2.817	

4.2.3 Operating current

Table 4-6 Operating current characteristics

Mode	Conditions	V_{DD} = 3.3V				Unit
		-40°C	25°C	85°C	105°C	
Run Mode	HCLK=120 MHz, 4 wait period for Flash read operation, APB clock is enabled (cache enable).	12.18	20.95	22.31	23.44	mA
	HCLK=120 MHz, 4 wait period for Flash read operation, APB clock is disabled (cache enable).	6.71	11.50	12.74	13.81	mA
	HCLK = HSE (8 MHz), 0 wait period for Flash read operation,	1.83	1.98	3.08	4.1	mA

Mode	Conditions	V_{DD} = 3.3V				Unit
		-40°C	25°C	85°C	105°C	
	APB clock is enabled (cache enable).					
	HCLK = HSE (8 MHz), 0 wait period for Flash read operation, APB clock is disabled (cache enable).	1.19	1.36	2.39	3.41	mA
	HCLK = LSI (40 kHz)	0.23	0.31	1.34	2.33	mA
	HCLK =LSE (32.768 kHz)	0.23	0.3	1.35	2.32	mA
Sleep Mode	HCLK = 120 MHz, APB clock is enabled	8.52	14.63	15.92	17.01	mA
	HCLK = 120 MHz, APB clock is disabled.	3.3	5.65	6.82	7.85	mA
	HCLK = HSI (8 MHz), APB clock is enabled.	1.56	1.69	2.95	3.72	mA
	HCLK = HSI (8 MHz), APB clock is disable.	0.88	1.01	2.85	3.04	mA
Stop Mode	LDO operates at full speed, HSE/HSI/LSE is disabled, IWDG is disabled.	202.67	303	1322	2179	µA
	LDO low-power state, HSE/HSI/LSE is disabled, IWDG is disabled.	18.38	89.47	729	1374	µA
Standby Mode	LSI and IWDG are enabled.	2.98	3.87	16.74	30.29	µA
	LSI and IWDG are disabled.	2.96	3.87	16.68	30.22	µA
	All oscillators are disabled.	2.35	3.36	16.16	29.72	µA

4.2.4 High-speed external (HSE) clock characteristics

HK32F103x8xBT6A integrates a HSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

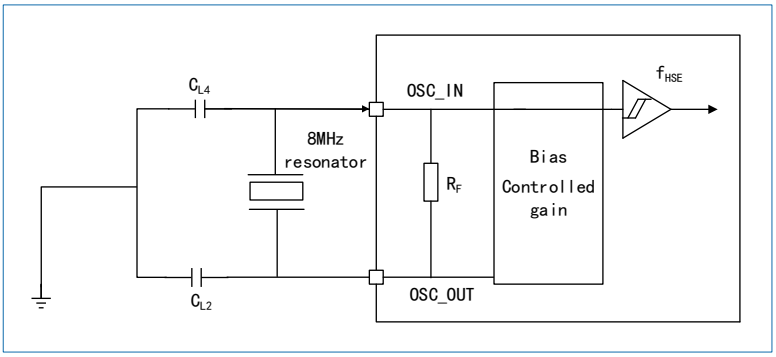

Figure 4-1 Typical application with HSE (8MHz)

HK32F103x8xBT6A can be clocked from the OSC_IN pin. The requirements of this clock signal are described as follows:

Table 4-7 HSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	1	8	25	MHz
V_{HSEH}	OSN_IN input pin high level voltage		0.7*V_{DD}	-	V_{DD}	V
V_{HSEL}	OSN_IN input pin low level voltage		V_{SS}	-	0.3*V_{DD}	

Symbol	Description	Conditions	Min	Typ	Max	Unit
$T_{w(HSE)}$	OSN_IN high or low time		5	-	-	ns
$T_{r(HSE)}/T_{f(HSE)}$	OSN_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSN_IN input capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

4.2.5 Low-speed external (LSE) clock characteristics

HK32F103x8xBT6A integrates an LSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

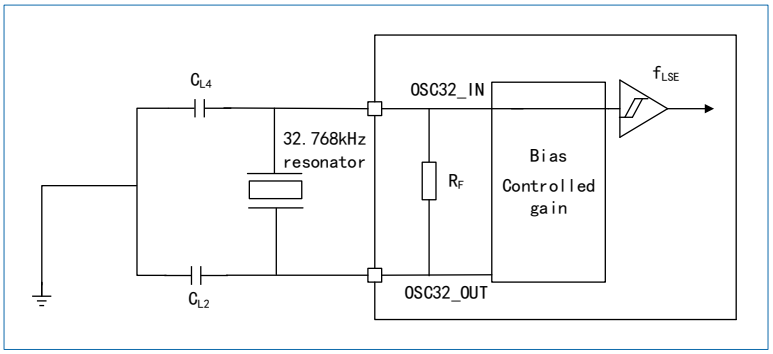

Figure 4-2 Typical application with LSE

HK32F103x8xBT6A can be clocked from the OSC32_IN pin. The requirements of this clock signal are described as follows:

Table 4-8 LSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{LSE_ext}	External clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSN32_IN input pin high level voltage		$0.7*V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSN32_IN input pin low level voltage		V_{SS}	-	$0.3*V_{DD}$	
$T_{w(LSE)}$	OSN32_IN high or low time		450	-	-	ns
$T_{r(LSE)}/T_{f(LSE)}$	OSN32_IN rise or fall time		-	-	50	
$C_{in(LSE)}$	OSN32_IN input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%

4.2.6 High-speed internal (HSI) RC oscillator

Table 4-9 HSI RC oscillator characteristics

Symbol	Description	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
$ACC_{(HSI)}$	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register		-1	-	1	
		Factory calibrated	TA= –40 ~ +105°C	-2	-	2.5	%
			TA= –40 ~ +85°C	-1.5	-	2.2	%
			TA= 0~ +70°C	-1.3	-	2	%
			TA= 25°C	-1.1	-	1.8	%
$Tsu_{(HSI)}$	HSI oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		1	-	2	µs
$IDD_{(HSI)}$	HSI oscillator power	-		-	80	100	µA

Symbol	Description	Conditions	Min	Typ	Max	Unit
	consumption					

4.2.7 Low-speed internal (LSI) RC oscillator

Table 4-10 LSI RC oscillator characteristics

Symbol	Description	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$T_{su(LSI)}$	LSI oscillator startup time	-	-	85	μs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	0.65	1.2	μA

4.2.8 PLL characteristics

Table 4-11 PLL characteristics

Symbol	Description	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL Input clock	1	8.0	25	MHz
	PLL input clock duty	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	96	MHz
t_{LOCK}	PLL Lock time	-	-	200	us
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.9 Flash memory characteristics

Table 4-12 Flash memory characteristics

Symbol	Description	Min	Typ	Max	Unit
T_{PROG}	A byte programming time	6	-	7.5	μs
T_{ERASE}	Page erase time	4	-	5	ms
	Mass erase time	30	-	40	ms
I_{DDPROG}	A byte programming current	-	-	5	mA
$I_{DDERASE}$	Sector/mass erase current	-	-	2	mA
I_{DDREAD}	Supply current@24MHz (read mode)	-	2	3	mA
	Supply current@1MHz (read mode)	-	0.25	0.4	mA
N_{END}	Endurance	100	-	-	kcycles
t_{RET}	Data retention	20	-	-	year
V_{prog}	Programming voltage	1.8	3.3	3.6	V

4.2.10 I/O port characteristics

Table 4-13 I/O static characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3V	1.6	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3V	-	-	1.5	V
V_{IHhys}	Input high level voltage	V_{DD} = 3.3V	1.56	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 3.3V	-	-	1.26	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3V	-	450	-	mV

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current Weak pull-up equivalent resistor	V_{DD} = 3.3V 0<V_{IN}<3.3V	-	-	1	μA
		V_{DD} = 3.3V V_{IN} = 5V	-	-	1	μA
R_{PU}	Weak pull-down equivalent resistor	V_{IN} = V_{SS}	-	35	-	KΩ
R_{PD}	I/O pin capacitance	V_{IN} = V_{DD}	-	35	-	KΩ
C_{IO}	Schmitt trigger voltage hysteresis	-	-	5	-	pF

4.2.11 Output voltage characteristics

Table 4-14 Output voltage DC characteristics

Mode	Symbol	Description	Conditions	Min	Max	Unit
10	V_{OL}	Input low level voltage	CL = 50pF, V_{DD} = 2V ~ 3.6V R_{Load} = 5 Kohm	-	2	MHz
	V_{OH}	Input high level voltage		-	125	ns
01	V_{OL}	Input low level voltage	CL = 50pF, V_{DD} = 2V ~ 3.6V R_{Load} = 5 Kohm	-	2	MHz
	V_{OH}	Input high level voltage		-	125	ns
11	V_{OL}	Input low level voltage	CL = 50pF, V_{DD} = 2V ~ 3.6V R_{Load} = 5 Kohm	-	2	MHz
	V_{OH}	Input high level voltage		-	125	ns

Table 4-15 Output voltage AC characteristics

Mode	Symbol	Description	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2V ~ 3.6V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2V ~ 3.6V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2V ~ 3.6V	-	50	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	5	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	5	ns

4.2.12 TIM timer characteristics

Table 4-16 TIM characteristics

Symbol	Description	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIM\ x\ CLK}$
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$F_{TIMxCLK}/2$ (1)	MHz
Res $_{TIM}$	Timer resolution	-	16	bit
Tcounter	16-bit counter clock period when selecting an internal clock	1	65536	$T_{TIM\ x\ CLK}$
T_{MAX_COUNT}	Maximum possible count	-	65536x65536	$T_{TIM\ x\ CLK}$

(1). $f_{TIM\ x\ CLK}$ = 120 MHz

4.2.13 ADC characteristics

Table 4-17 ADC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	ADC power supply	-	2	3.3	3.6	V
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Reference input current	-	-	150	480	μA
INL	Integral nonlinearity (The max result of the actual conversion point subtracting the actual conversion line)	f_{ADC}=14MHz; RAIN<10KΩ; Test after calibration: V_{DDA}=2.4~3.6V.	-	±1.5	±4	LSB
DNL	Differential nonlinearity (Max conversion error)	f_{ADC}=14MHz; RAIN<10KΩ; Test after calibration: V_{DDA}=2.4~3.6V.	-	±1	±3	LSB
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (VssA or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	-	5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 14 MHz	5.9			μs
			83			$1/f_{ADC}$
t_{lat}	Injected trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	μs
			-	-	3	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	μs
			-	-	2	$1/f_{ADC}$
t_S	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	μs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	0	0	1	μs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	μs
			14 to 252 (t_s for sampling, +12.5 for successive approximation)			$1/f_{ADC}$

4.2.14 Temperature sensor characteristics

Table 4-18 Temperature sensor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Avg_Slope	Average slope	2.9	3	3.1	mV/℃

5 Pinouts and pin descriptions

To meet different environment requirements, HK32F103x8xBT6A is offered in three packages: LQFP64/ LQFP64/LQFP48.

5.1 LQFP100

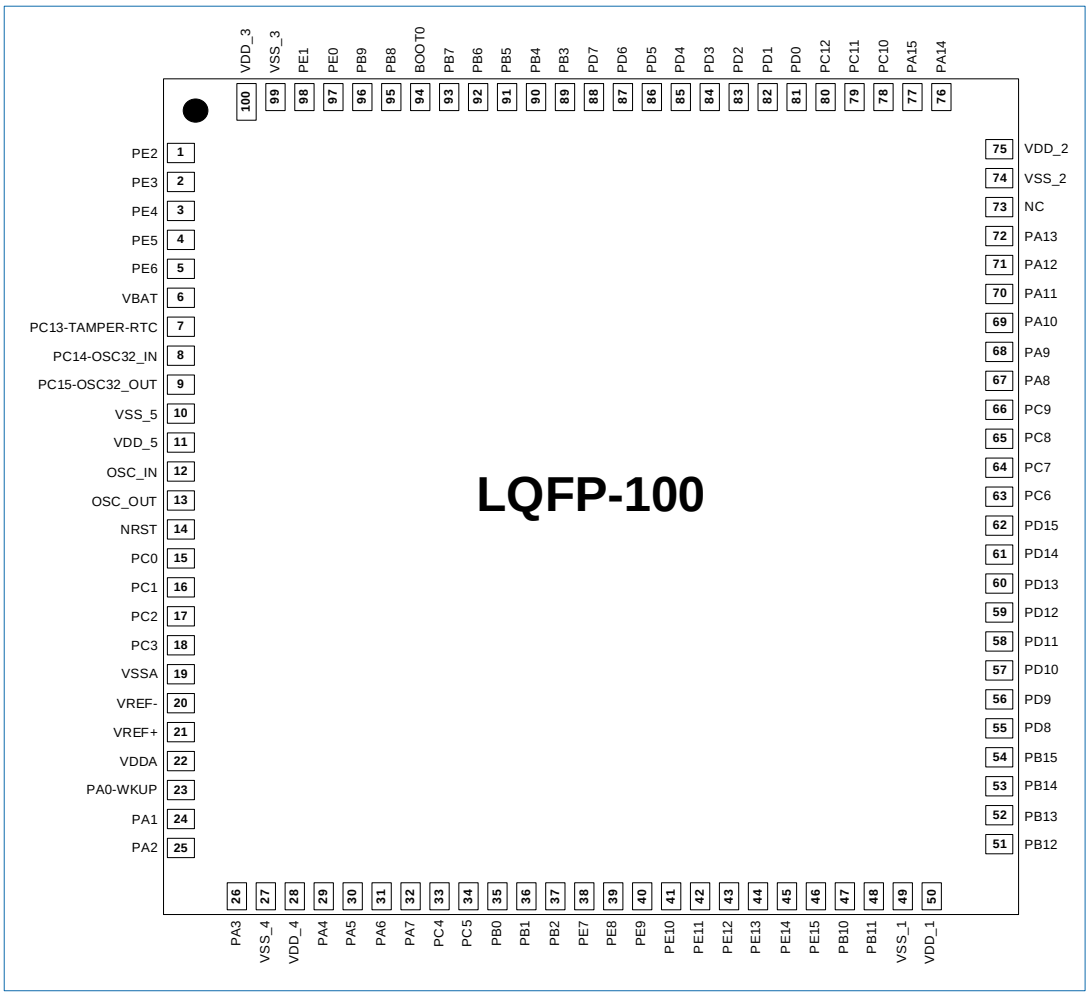

Figure 5-1 LQFP100 package pinout

5.2 LQFP64

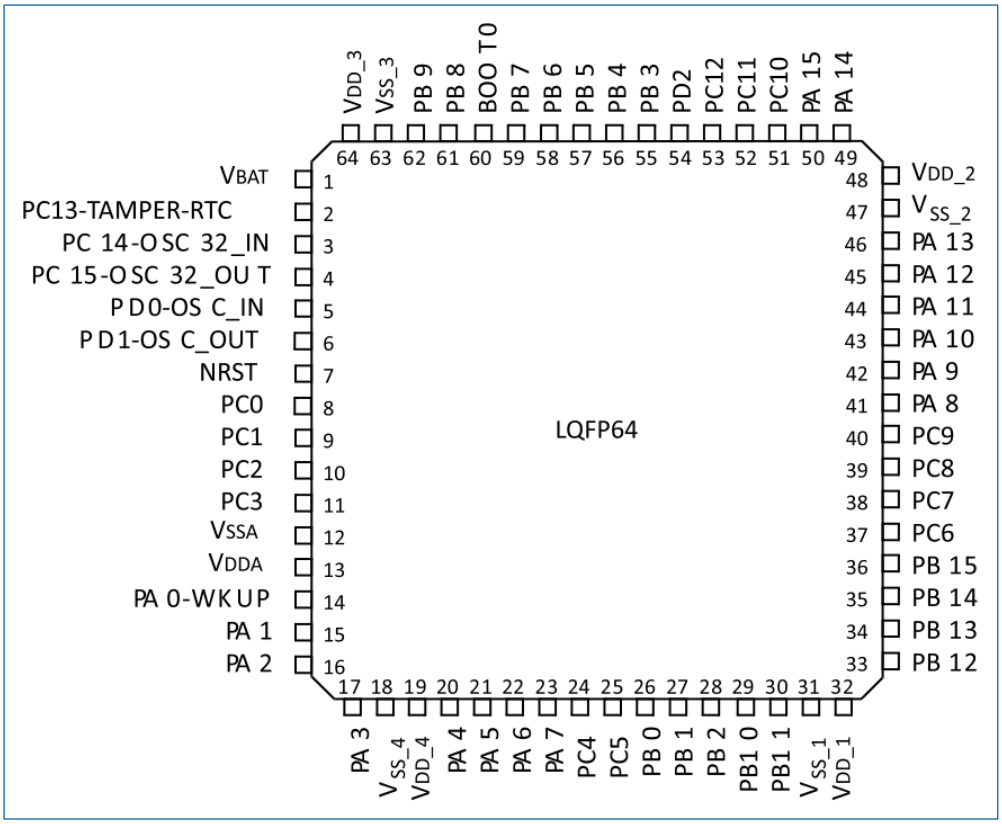

Figure 5-2 LQFP64 package pinout

5.3 LQFP48

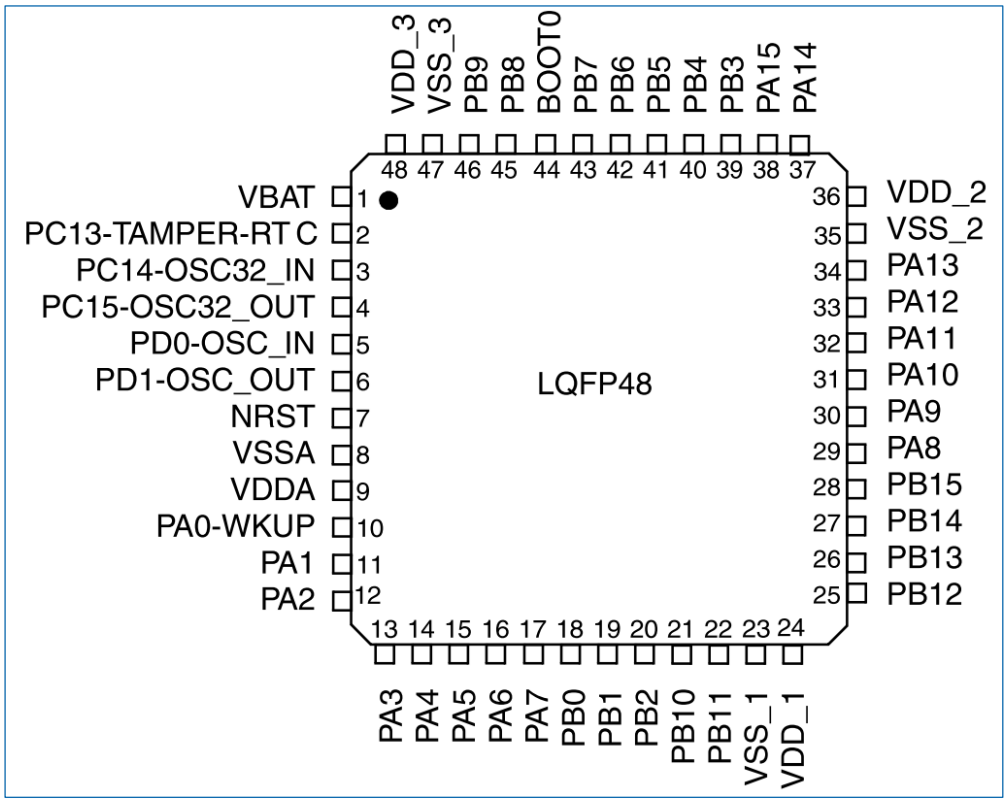

Figure 5-3 LQFP48 package pinout

5.4 Pin description

Table 5-1 shows pin description of LQFP100, LQFP64 and LQFP48 package.

Table 5-1 LQFP100/LQFP64/LQFP48 package pin description

LQFP48	LQFP64	LQFP100	Pin Name	Type(1)	I/O Level(2)	Main function	Alternative Function	
							Default Function	Remap Function
-	-	1	PE2	I/O	-	PE2	TRACECKO	TXEV/EXTIN2
-	-	2	PE3	I/O	-	PE3	TRACED0	TXEV/EXTIN3
-	-	3	PE4	I/O	-	PE4	TRACED1	TXEV/EXTIN4
-	-	4	PE5	I/O	-	PE5	TRACED2	TXEV/EXTIN5
-	-	5	PE6	I/O	FT	PE6	TRACED3	TXEV/EXTIN6
1	1	6	VBAT	S	-	VBAT	-	-
2	2	7	PC13-TAMPER-RTC	I/O(3)	-	PC13	TAMPERIN/WKUP1/RTCO	TXEV/EXTIN13
3	3	8	PC14-OSC32_IN	I/O(3)	-	PC14	OSC32_IN/LSE_CKI	TXEV/EXTIN14
4	4	9	PC15-OSC32_OUT	I/O(3)	-	PC15	OSC32_OUT	TXEV/EXTIN15
-	-	10	VSS_5	S	-	VSS_5	-	-
-	-	11	VDD_5	S	-	VDD_5	-	-
5	5	12	OSC_IN	I	-	OSC_IN	OSC_IN/HSE_CKI	TXEV/PD0[2] EXTIN0[2]
6	6	13	OSC_OUT	O	-	OSC_OUT	OSC_OUT	TXEV/PD1[2] EXTIN1[2]
7	7	14	NRST	I/O	-	NRST	-	-
-	8	15	PC0	I/O	-	PC0	ADC12_IN10	TXEV/EXTIN0
-	9	16	PC1	I/O	-	PC1	ADC12_IN11	TXEV/EXTIN1
-	10	17	PC2	I/O	-	PC2	ADC12_IN12	TXEV/EXTIN2
-	11	18	PC3	I/O	-	PC3	ADC12_IN13	TXEV/EXTIN3
8	12	19	VSSA	S	-	VSSA	-	-
-	-	20	VREF-	S	-	VREF-	-	-
-	-	21	VREF+	S	-	VREF+	-	-
9	13	22	VDDA	S	-	VDDA	-	-
10	14	23	PA0-WKUP	I/O(3)	-	PA0	WKUP0/USART2_CTS/ADC12_IN0 TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR/EXTIN0	TXEV
11	15	24	PA1	I/O	-	PA1	USART2_RTS/ADC12_IN1 TIM5_CH2/TIM2_CH2/EXTIN1/ RCC_CKI0	TXEV

LQFP48	LQFP64	LQFP100	Pin Name	Type[1]	I/O Level[2]	Main function	Alternative Function	
							Default Function	Remap Function
12	16	25	PA2	I/O	-	PA2	USART2_TX/TIM5_CH3 ADC12_IN2/TIM2_CH3/EXTIN2	TXEV
13	17	26	PA3	I/O	-	PA3	USART2_RX/TIM5_CH4 ADC12_IN3/TIM2_CH4/EXTIN3	TXEV
-	18	27	VSS_4	S	-	VSS_4	-	-
-	19	28	VDD_4	S	-	VDD_4	-	-
14	20	29	PA4	I/O	-	PA4	SPI1_NSS/USART2_CK /ADC12_IN4/EXTIN4	TXEV
15	21	30	PA5	I/O	-	PA5	SPI1_SCK/ADC12_IN5 /EXTIN5	TXEV
16	22	31	PA6	I/O	-	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1/EXTIN6	TXEV/TIM1_BKIN
17	23	32	PA7	I/O	-	PA7	SPI1_MOSI/ADC12_IN7/TIM3_CH2/EXTIN7	TXEV/TIM1_CH1N
-	24	33	PC4	I/O	-	PC4	ADC12_IN14	TXEV/EXTIN4
-	25	34	PC5	I/O	-	PC5	ADC12_IN15	TXEV/EXTIN5
18	26	35	PB0	I/O[3]	-	PB0	ADC12_IN8/TIM3_CH3	TXEV/TIM1_CH2N/EXTIN0
19	27	36	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4 RCC_CKI1	TXEV/TIM1_CH3N/EXTIN1
20	28	37	PB2	I/O	FT	PB2	BOOT1	TXEV/EXTIN2
-	-	38	PE7	I/O	FT	PE7	-	TXEV/TIM1_ETR/EXTIN7
-	-	39	PE8	I/O	FT	PE8	-	TXEV/TIM1_CH1N/EXTIN8
-	-	40	PE9	I/O	FT	PE9	-	TXEV/TIM1_CH1/EXTIN9
-	-	41	PE10	I/O	FT	PE10	-	TXEV/TIM1_CH2N/EXTIN10
-	-	42	PE11	I/O	FT	PE11	-	TXEV/TIM1_CH2/EXTIN11
-	-	43	PE12	I/O	FT	PE12	-	TXEV/TIM1_CH3N/EXTIN12
-	-	44	PE13	I/O	FT	PE13	-	TXEV/TIM1_CH3/EXTIN13
-	-	45	PE14	I/O	FT	PE14	-	TXEV/TIM1_CH4/EXTIN14
-	-	46	PE15	I/O	FT	PE15	-	TXEV/TIM1_BKIN/EXTIN15
21	29	47	PB10	I/O	-	PB10	I2C2_SCL/USART3_TX	TXEV/TIM2_CH3/EXTIN10
22	30	48	PB11	I/O	-	PB11	I2C2_SDA/USART3_RX	TXEV/TIM2_CH4/EXTIN11
23	31	49	VSS_1	S	-	VSS_1	-	-
24	32	50	VDD_1	S	-	VDD_1	-	-
25	33	51	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/USART3_CK/TIM1_BKIN	TXEV/EXTIN12

LQFP48	LQFP64	LQFP100	Pin Name	Type(1)	I/O Level(2)	Main function	Alternative Function	
							Default Function	Remap Function
26	34	52	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/TIM1_CH1N	TXEV/EXTIN13
27	35	53	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N/USART3_RTS	TXEV/EXTIN14
28	36	54	PB15	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N	TXEV/EXTIN15
-	-	55	PD8	I/O	FT	PD8	-	TXEV/USART3_TX/EXTIN8
-	-	56	PD9	I/O	FT	PD9	-	TXEV/USART3_RX/EXTIN9
-	-	57	PD10	I/O	FT	PD10	-	TXEV/USART3_CK/EXTIN10
-	-	58	PD11	I/O	FT	PD11	-	TXEV/USART3_CTS/EXTIN11
-	-	59	PD12	I/O	FT	PD12	-	TXEV/TIM4_CH1/USART3_RTS/EXTIN12
-	-	60	PD13	I/O	FT	PD13	-	TXEV/TIM4_CH2/EXTIN13
-	-	61	PD14	I/O	FT	PD14	-	TXEV/TIM4_CH3/EXTIN14
-	-	62	PD15	I/O	FT	PD15	-	TXEV/TIM4_CH4/EXTIN15
-	37	63	PC6	I/O	FT	PC6	-	TXEV/TIM3_CH1/EXTIN6
-	38	64	PC7	I/O	FT	PC7	-	TXEV/TIM3_CH2/EXTIN7
-	39	65	PC8	I/O	FT	PC8	-	TXEV/TIM3_CH3/EXTIN8
-	40	66	PC9	I/O	FT	PC9	-	TXEV/TIM3_CH4/EXTIN9
29	41	67	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/MCO/EXTIN8	TXEV
30	42	68	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2/EXTIN9	TXEV
31	43	69	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3/EXTIN10	TXEV
32	44	70	PA11	I/O	FT	PA11	USART1_CTS/USBDM/CAN1_RX/TIM1_CH4/EXTIN11	TXEV
33	45	71	PA12	I/O	FT	PA12	USART1_RTS/USBDP/CAN1_TX/TIM1_ETR/EXTIN12	TXEV
34	46	72	PA13	I/O	FT	JTMS-SWDIO		PA13 TXEV
-	-	73	NC	-	-	-	-	-
35	47	74	VSS_2	S		VSS_2	-	-
36	48	75	VDD_2	S		VDD_2	-	-
37	49	76	PA14	I/O	FT	JTCK-SWCLK	EXTIN14	TXEV/PA14
38	50	77	PA15	I/O	FT	JTDI	EXTIN15	TXEV/TIM2_CH1_ETR/PA15/SPI1_NSS
-	51	78	PC10	I/O	-	PC10	-	TXEV/USART3_TX/EXTIN10
-	52	79	PC11	I/O	-	PC11	-	TXEV/USART3_RX/EXTIN11
-	53	80	PC12	I/O	-	PC12	-	TXEV/USART3_CK/EXTIN12
-		81	PD0	I/O	FT	OSC_IN	-	TXEV/CAN1_RX/EXTIN0
		82	PD1	I/O	FT	OSC_OUT	-	TXEV/CAN1_TX/EXTIN1

LQFP48	LQFP64	LQFP100	Pin Name	Type(1)	I/O Level(2)	Main function	Alternative Function	
							Default Function	Remap Function
-	54	83	PD2	I/O	-	PD2	TIM3_ETR	TXEV/EXTIN2
-	-	84	PD3	I/O	FT	PD3	-	TXEV/USART2_CTS/EXTIN3
-	-	85	PD4	I/O	FT	PD4	-	TXEV/USART2_RTS/EXTIN4
-	-	86	PD5	I/O	FT	PD5	-	TXEV/USART2_TX/EXTIN5
-	-	87	PD6	I/O	FT	PD6	-	TXEV/USART2_RX/EXTIN6
-	-	88	PD7	I/O	FT	PD7	-	TXEV/USART2_CK/EXTIN7
39	55	89	PB3	I/O	-	JTDO	-	TXEV/PB3/TRACESWO/TIM2_CH2/SPI1_SCK/EXTIN3
40	56	90	PB4	I/O	-	NJTRST	-	TXEV/PB4/TIM3_CH1/SPI1_MISO/EXTIN4
41	57	91	PB5	I/O	-	PB5	I2C1_SMBA	TXEV/TIM3_CH2/SPI1_MOSI/EXTIN5
42	58	92	PB6	I/O	-	PB6	I2C1_SCL/TIM4_CH1	TXEV/USART1_TX/EXTIN6
43	59	93	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/RCC_CKI3	TXEV/USART1_RX/EXTIN7
44	60	94	BOOT0	I	-	BOOT0	-	-
45	61	95	PB8	I/O	-	PB8	TIM4_CH3	TXEV/I2C1_SCL/CAN1_RX/EXTIN8
46	62	96	PB9	I/O	-	PB9	TIM4_CH4	TXEV/I2C1_SDA/CAN1_TX/EXTIN9
-	-	97	PE0	I/O	FT	PE0	TIM4_ETR	TXEV/EXTIN0
-	-	98	PE1	I/O	FT	PE1	-	TXEV/EXTIN1
47	63	99	VSS_3	S	-	VSS_3	-	-
48	64	100	VDD_3	S	-	VDD_3	-	-

(1). I= input, O=output, I/O= input/output, S=supply.

(2). FT: 5V tolerant.

(3). Except for these I/Os， all I/Os support Schmitt trigger function by configuring corresponding registers.

6 Package characteristics

6.1 LQFP100

LQFP100 is a 14 x 14 mm and 0.5 mm pitch package.

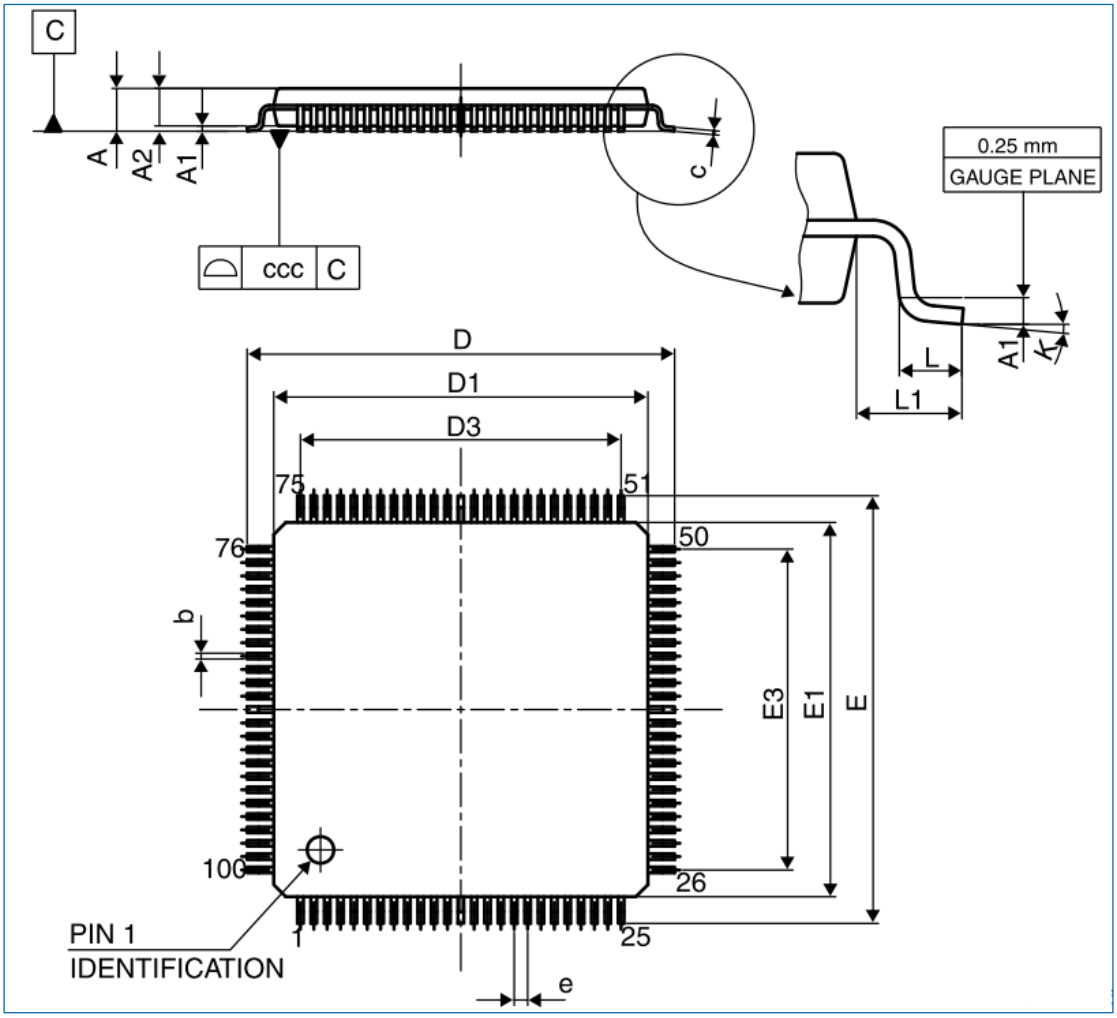

Figure 6-1 LQFP100 package outline

Table 6-1 LQFP100 package parameters

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

6.1.1 Recommended footprint

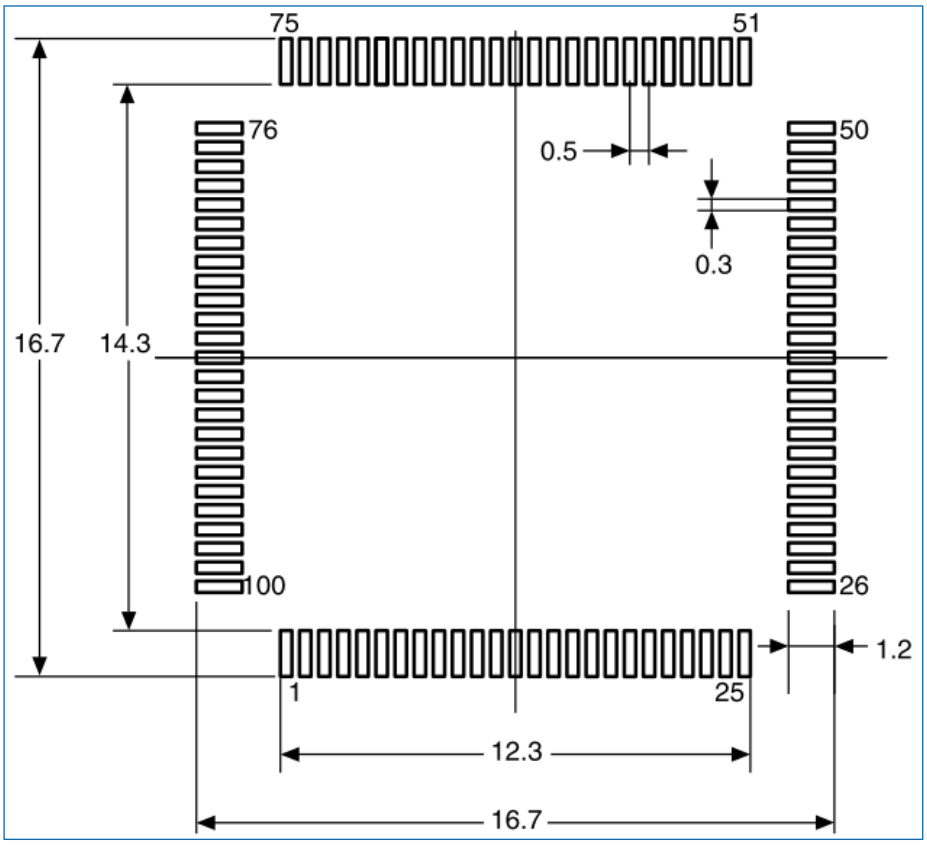

Figure 6-2 LQFP100 recommended footprint

The measurement unit in the figure is millimeter (mm).

6.2 LQFP64

LQFP64 is a 10 x 10 mm and 0.5 mm pitch package.

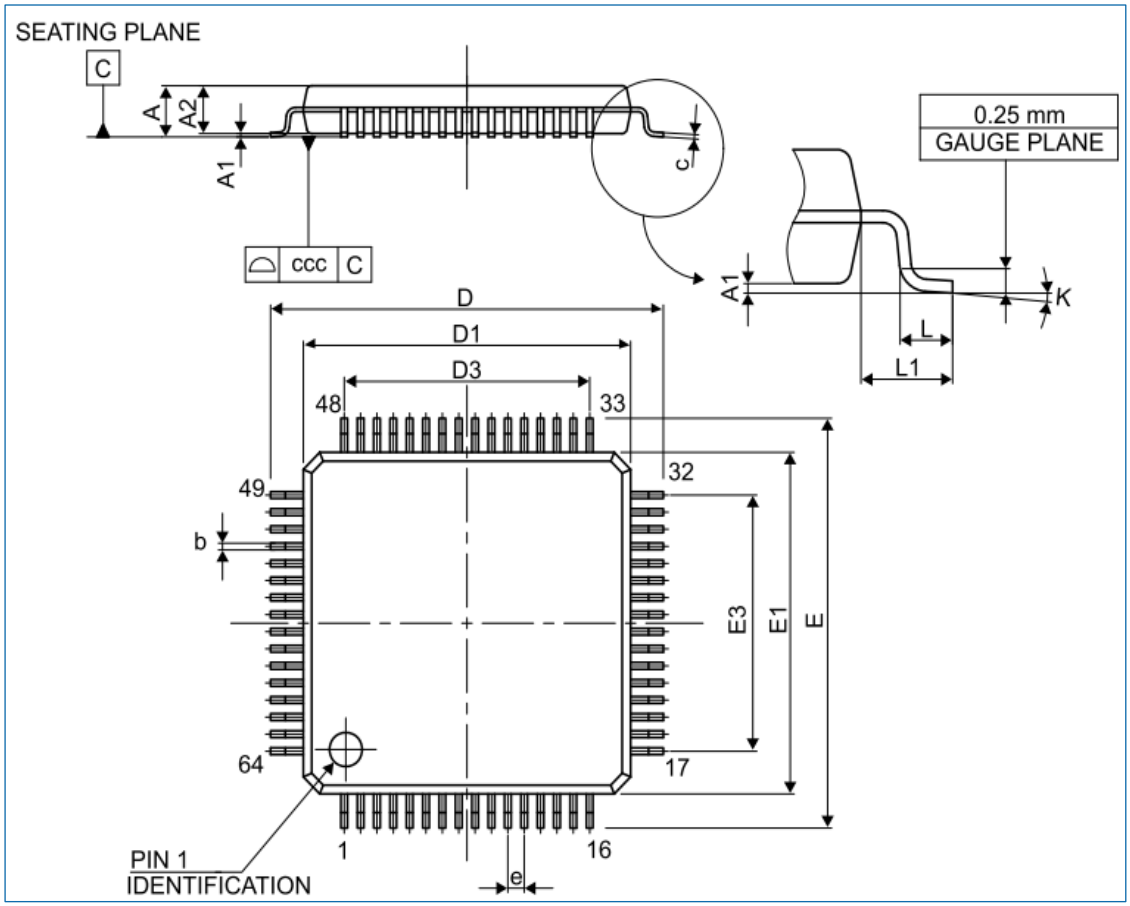

Figure 6-3 LQFP64 package outline

The measurement unit in the figure is millimeter (mm).

Table 6-2 LQFP64 package parameters

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

(2). Values in inches are converted from mm and rounded to 4 decimal digits.

6.2.1 Recommended footprint

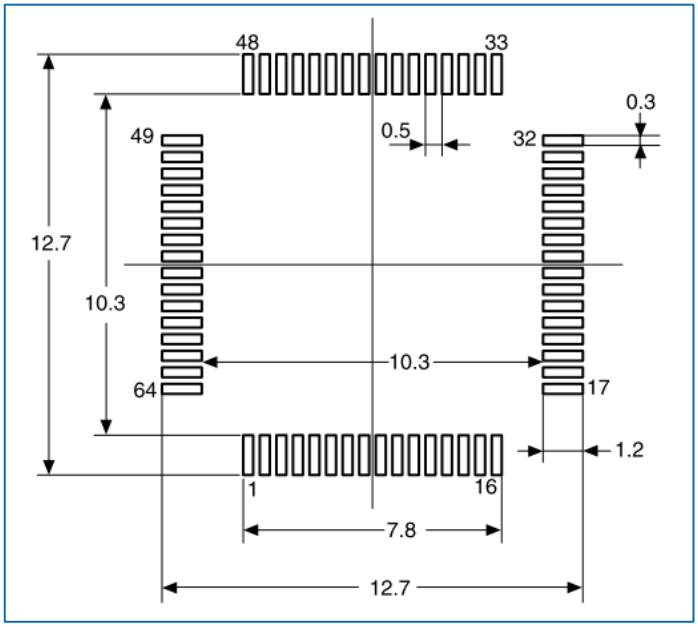

Figure 6-4 LQFP64 recommended footprint

The measurement unit in the figure is millimeter (mm).

6.3 LQFP48

LQFP48 is a 7 mm x 7 mm and 0.5 mm pitch package.

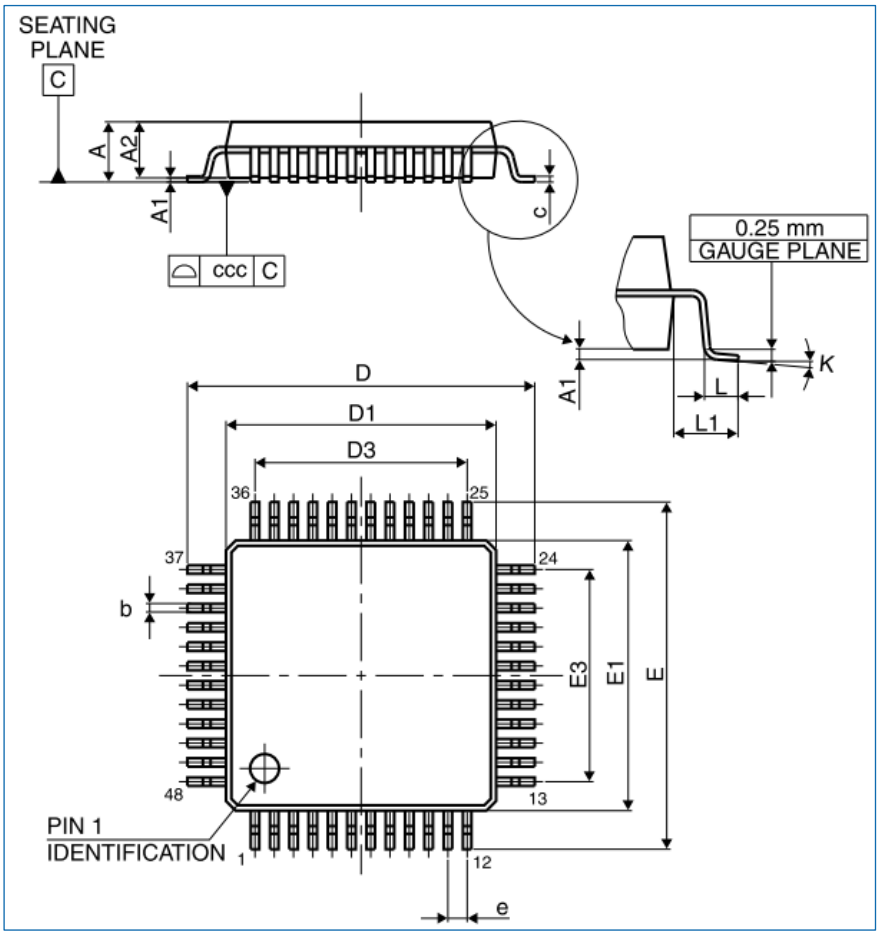

Figure 6-5 LQFP48 package outline

Table 6-3 LQFP48 package parameters

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

6.3.1 Recommended footprint

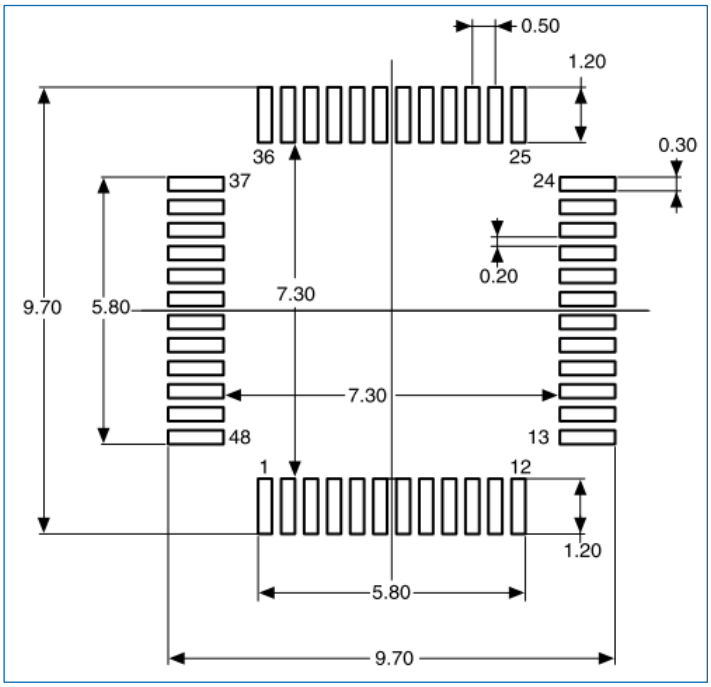

Figure 6-6 LQFP48 recommended footprint

The measurement unit in the figure is millimeter (mm).

7 Ordering information

Table 7-1 HK32F103x8xBT6A ordering information

Package	HK32F103x8xBT6A series	Packaging	Comments
LQFP48	HK32F103C8T6A	Tape and reel/Tray	-
	HK32F103CBT6A	Tape and reel/Tray	-
LQFP64	HK32F103R8T6A	Tape and reel/Tray	-
	HK32F103RBT6A	Tape and reel/Tray	-
LQFP100	HK32F103V8T6A	Tape and reel/Tray	
	HK32F103VBT6A	Tape and reel/Tray	

8 Glossary and Abbreviations

Name	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-Wakeup
CRC	Cyclic Redundancy Check
CSS	Clock Security System
DMA	Direct Memory Access
EXTI	Extended Interrupts and Events Controller
FSMC	Flexible Static Memory Controller
GPIO	General Purpose Input Output
HSE	High Speed External (Clock Signal)
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-Speed Internal (Clock Signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-Down Reset
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous Asynchronous Receiver Transmitter
WWDG	Window Watchdog

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