HK32F103xCxDxE Datasheet

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Preface

Purpose

This document introduces the block diagram, the memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F103xCxDxE Series SOC, to help users quickly understand its features and functions.

Audience

This document is intended for:

- HK32F103xCxDxE Developer
- HK32F103xCxDxE Tester
- HK32F103xCxDxE user

Release Notes

This document is corresponding to HK32F103xCxDxE Series SOC.

Revision History

Version	Date	Description
1.0.0	2019/07/23	Initial release
1.0.1	2020/03/04	Update *Section 3.13 Low-power modes.*
1.0.2	2020/03/09	Update *Section 4.2.5 Operating current*.
1.0.3	2020/06/19	Update *Section 3.9.2 clock tree.*
1.0.4	2020/07/03	Update *Section 4.2.12 Flash memory characteristics.*
1.0.5	2020/10/12	Update *Section 3.29 ADC*.
1.1.0	2021/03/18	Update *Section 4.2.17 ADC characteristics.*
1.1.4	2021/06/01	Update *Section 4.2.17 ADC characteristics.*
1.1.5	2021/06/23	Update *Section 4.2.5 Operating current.*
1.1.6	2021/07/15	Update Section *4.2.17 DAC characteristics*

Contents

1 Introduction

This document is the datasheet for HK32F103xCxDxE series System-on-Chips (SOCs). HK32F103xCxDxE is a family of low-power microcontrollers (MCU) developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd, including:

HK32F103xC:

- HK32F103RCT6
- HK32F103VCT6

HK32F103xD:

- HK32F103RDT6
- HK32F103VDT6

HK32F103xE:

- HK32F103RET6
- HK32F103VET6

Please refer to HK32F103xCxDxE Reference Manual for more details.

2 Product overview

Based on ARM® Cortex®-M3 core, HK32F103xCxDxE embeds large capacity memories, including a 527-Kbyte Flash, a 64-Kbyte SRAM. Its maximum frequency is 120 MHz. It can connect to an external storage device (NOR/PSRAM/NAND/PC Card) with 1-Gbyte capacity via a flexible static memory controller (FSMC) module, 256-Mbyte capacity of which is used to store instructions or for the internal 1 kbytes instruction cache.

HK32F103xCxDxE embeds a CRC module for data integrity verification.

HK32F103xCxDxE integrates rich communications interfaces to meet multiple communications applications needs, including: 5 USARTs, 3 SPIs (supports the I2S protocol), 1 SDIO, 2 I2Cs, 1 CAN 2.0A/2.0B and 1 Full-speed (FS) USB device.

HK32F103xCxDxE embeds 2 advanced 16-bit PWM timers (total 8 PWM output channels, 6 of which have complementary PWM output with programmable inserted dead-times), and 4 general-purpose 16-bit PWM timers (total 16 PWM output channels).

HK32F103xCxDxE provides an independent V_{BAT} power domain. When the main power V_{DD} is powered down, the RTC module continues to operate with V_{BAT} power supply. Backup registers with 20 bytes and a 512-Byte SRAM are available in the V_{BAT} power domain (a 512-Byte SRAM is not available in sample ICs).

HK32F103xCxDxE integrates rich analog circuits: three 12-bit ADCs (total 25 analog signal input channels, of which 2 channels for weak driven signal inputs and 1 channel for 5V high-level voltage signal input), two 12-bit DACs, one temperature sensor, one 0.8V internal reference voltage, one low-voltage detector (LVD), one POR/PDR circuit, and one V_{BAT} voltage divider (the output of divider connects to ADC on-chip).

HK32F103xCxDxE supports multiple power consumption modes. In the lowest power consumption mode, the typical leakage current is less than 100 nA.

HK32F103xCxDxE operates in the -40°C to +105°C temperature range, from a 2.0 to 3.6 V power supply. It meets the environment requirement of most applications.

The whole HK32F103xC, HK32F103xD and HK32F103xE series products offer 64-pin and 100-pin packages. Depending on the package chosen, different sets of peripherals are included.

With its various peripheral interfaces, HK32F103xCxDxE is suitable for a wide range of applications:

- Industry application, such as programmable controllers, printers, and scanners
- Human-machine audio-video multimedia interaction
- Graph-displaying devices
- Speech recognition devices
- Safety monitoring equipment
- Motor drive and speed control
- Low-power terminals with sensors for Internet of Things
- UAV flight control, pylon control
- Toy products
- Household appliances
- Intelligent robots
- Smart watches and sports bracelets

2.1 Features

- CPU core

- ARM® Cortex®-M3 core
- Maximum frequency: 120 MHz
- 24-bit SysTick timer
- Supports interrupt vector remapping (through configuring Flash registers)

- Operating voltage range
  - Main power supply (V_{DD}): 1.8 V to 3.6 V
  - Back-up power supply (V_{BAT}): 1.8 V to 3.6 V
  - When the main power is powered down, the RTC module continues to operate with V_{BAT} supply.
  - When the main power is powered down, V_{BAT} supply provides backup registers with 20 bytes.
- Operating temperature range: -40°C to +105°C
- Typical operating current (V_{DD})
  - Run mode: 10.44mA@102MHz@3.3V
  - Sleep mode: 5.65mA@102MHz@3.3V
  - Stop mode: 89.47μA@3.3V
  - Standby mode: 3.36μA@3.3V
- Typical operating current (V_{BAT})
  - V_{BAT} RTC-on mode: 2.67μA @3.3V
  - V_{BAT} RTC-off mode: 2.19μA @3.3V
- Memory
  - 527 Kbytes Flash includes a 512-Kbyte main Flash block and a 15-Kbyte Information block.
  - When the CPU frequency is not more than 24 MHz, MCU supports 0 wait bus period.
  - Flash data security protection function (read or write protection can be set respectively).
  - A 1-Gbyte external storage device (NOR/PSRAM/NAND/PC Card) via a FSMC module (256-Mbyte block is used for instruction storage).
  - Up to 65-Kbyte internal SRAM (one 64-Kbyte SRAM, two 512-byte RAMs shared by all peripherals).
- DMA controller
  - 2 independent DMA controllers: DMA1 and DMA2
  - DMA1 provides 7 channels
  - DMA2 provides 5 channels
  - Supports multiple peripherals triggering: timer, ADC, SPI, I2C, USART.
- Data security
  - CRC32 verification hardware unit
- Clock
  - External high-speed clock (HSE): 4-32 MHz (typical value: 8 MHz)
  - External low-speed clock (LSE): 32.768 kHz
  - Internal high-speed clock (HSI): 56 MHz/8 MHz
  - Internal low-speed clock (LSI): 40 kHz
  - PLL clock
- Reset
  - External pin reset
  - POR/PDR reset
  - Software reset

- Watchdog timer reset (IWDG and WWDG)
- Low-power mode reset

- GPIO
  - Up to 51 GPIOs for 64-pin package / 80 GPIOs for 100-pin package
  - Each GPIO can be used as an external interrupt input
  - Built-in switchable pull-up/pull-down resistors
  - Supports Open-drain output
  - Supports Schmitt trigger voltage hysteresis input
  - Ultra-high/high/medium/low level output drive capacity is configurable.
  - Provides up to 20 mA driving current
- Data communications interfaces
  - 5 x USARTs
  - 3 x SPIs (supports the I2S protocol)
  - 2 x I2Cs
  - 1 x SDIO
  - 1 x CAN 2.0A/2.0B
  - 1 x FS USB
- Timer and PWM generator
  - 2 x advanced PWM timers: TIM1/TIM8 (total 8 PWM output channels, 6 of which have complementary PWM output with programmable inserted dead-times.)
  - 4 x general-purpose PWM timers: TIM2/TIM3/TIM4/TIM5 (total 16 PWM output channels)
  - 2 x basic timers: TIM6/TIM7 (supports CPU interrupts, DMA requests and DAC conversion trigger)
- RTC clock counter cooperates with the software to provide a clock-calendar function.
- Low-voltage detection
  - Adjustable 8 level thresholds of detecting voltage
  - Configurable rising edge and falling edge for detecting
- On-chip analog circuits
  - 3 x 12-bit ADCs up to 3 Msps (25 analog input channels in total: of which, 2 channels for weak driven signal inputs, 1 channel for a 5V high-level voltage signal input)
  - 2 x 12-bit DACs
  - 1 x temperature sensor
  - 1 x 0.8V internal reference voltage
  - 1 x V_{BAT} voltage divider (the divider output connects to internal ADC to monitor V_{BAT})
- ID
  - 96-bit unique ID (UID)
  - Each HK32F103xCxDxE provides a 96-bit UID.
- CPU trace and debug
  - SW-DP dual-wire debug interface
  - ARM® CoreSight™ debug component (DWT, FPB, ITM, TPIU)
  - Single-wire asynchronous trace data output interface (TRACESWO)
  - Four-wire synchronous trace data output interface (TRACEDO[3:0], TRACECK)
  - Customized DBGMCU debug controller (low-power mode simulation control, the debug peripheral

clock control, and debug and track interfaces allocation)

- Reliability
  - Passed HBM2000V/CDM500V/MM200V/LU level tests.

2.2 Device overview

Table 2-1 HK32F103xCxDxE series features

Features	HK32F103RCT6	HK32F103RDT6	HK32F103RET6	HK32F103VCT6	HK32F103VDT6	HK32F103VET6
Operating voltage	1.8 V ~ 3.6 V					
Operating temperature	-40°C ~ +105°C					
CPU frequency	120 MHz					
SysTick	1					
Flash (Kbyte)	256	384	512	256	384	512
SRAM (Kbyte)	65					
DMA	2					
CRC32	1					
FSMC	-	-	-	1	1	1
SDIO	1					
IWDG	1					
WWDG	1					
USART	5					
I2C	2					
USB	1					
CAN	1					
SPI/I2S	3					
Advanced PWM timer	2					
General-purpose PWM timer	4					
Basic timer	2					
GPIO	51			80		
ADC	3					
DAC	2					
PVD	1					
Temperature sensor	1					
96-bit UID	1					
Package	LQFP64			LQFP100		

256-Mbyte capacity of which is used to store instructions or for the internal 1 kbytes instruction cache.

3 Function description

3.1 Block diagram

ARM® Cortex®-M3 is a 32-bit RISC processor, which provides a MCU platform with low-cost, high-performance and low-power consumption features. It delivers outstanding computational performance and advanced system response to interrupts. With embedded ARM Cortex-M3 core, HK32F103xCxDxE family is compatible with ARM tools and software.

The block diagram of HK32F103xCxDxE shows as follows:

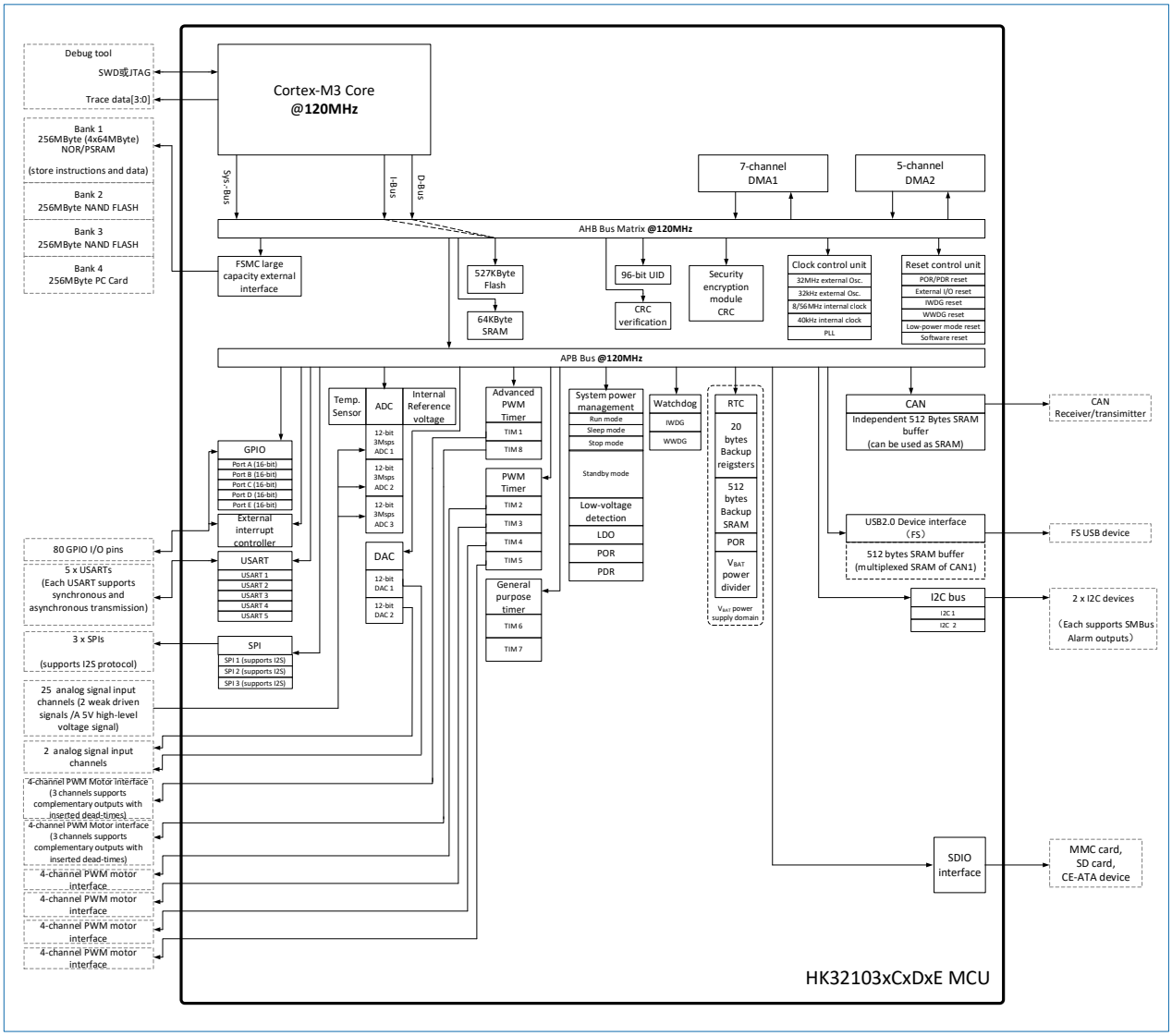

Figure 3-1 HK32F103xCxDxE block diagram

3.2 Memory mapping

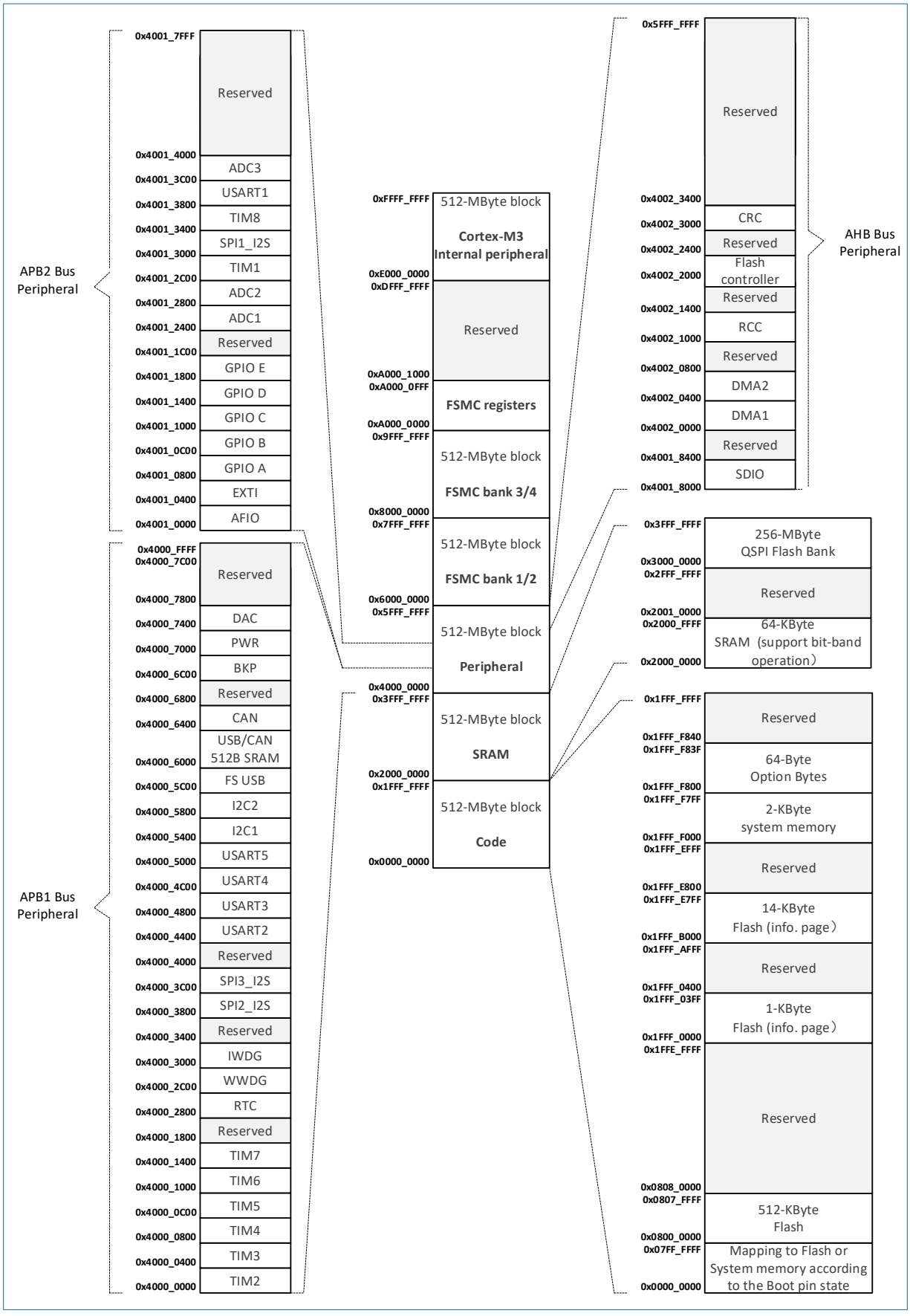

Figure 3-2 Memory mapping

3.2.1 Flash features

HK32F103xCxDxE integrates a Flash memory up to 527 Kbytes to store programs and data. The Flash consists of a main Flash block and an information block.

- Flash data width: 128 bits
- 2 Kbytes per page and 1 Kbyte per sector
- Flash access: write in a unit of half-word (16 bits), word (32 bits), two words (64 bits) and four words (128 bits); read in a unit of 128 bits
- Supports Flash read/write protection
- Supports pre-fetch instruction buffer and data buffer.

HK32F103xCxDxE integrates a module for encrypting and decrypting Flash. It supports automatic encrypting and decrypting to protect intellectual property (IP) on-chip.

Table 3-1 Flash features

Operation time	Read operation	Erase/write operation
	● 0 wait state, if HCLK ≤ 24 MHz ● 1 wait state, if 24 MHz <HCLK ≤ 48 MHz ● The number of wait state plus 1 when HCLK frequency increases 24 MHz.	● Write: about 42 µs (the time of writing a half-word, a word, two words or four words are the same) ● Flash page erase: 60 ms (min) ● Flash mass erase: 60 ms (min)
Operation voltage	2.0 V – 3.6 V	
Operation current	Write operation: about 6 mA Erase operation: about 2.2 mA	
Endurance	Supports about 100,000 cycles erase, read and write operations in total.	

3.2.2 Flash Option Word

Table 3-2 Flash Option Word

Address	[31:24]	[23:16]	[15:8]	[7:0]
0x1FFF_F800	nUSER	USER	nRDP	RDP
0x1FFF_F804	nDATA1	DATA1	nDATA0	DATA0
0x1FFF_F808	nWRP1	WRP1	nWRP0	WRP0
0x1FFF_F80C	nWRP3	WRP3	nWRP2	WRP2
0x1FFF_F810 - 0x1fff_f81f	Reserved			
0x1fff_f820	ENCRY_CFG[31:0]			
0x1fff_f824	DECRY_CFG[31:0]			
0x1fff_f828	UKEY[31:0]			
0x1fff_f82c	UKEY[63:32]			
0x1fff_f830	Reserved			IWDG_RL_IV[11:0]
0x1fff_f834	IWDG_INI_KEY[31:0]			
0x1fff_f838	LSI_LP_CTL[31:0]			
0x1fff_f83c	DBG_CLK_CTL[31:0]			

- ENCRY_CFG[31:0]: If the value of ENCRY_CFG equals to 0x1357_eca8，the Flash data encryption function is enabled. After it is enabled, writing data into the Flash and the data will be converted into ciphertext stored in the Flash.
- DECRY_CFG[31:0]: If the value of DECRY_CFG equals to 0x2468_db97，the Flash data decryption function

is enabled. After it is enabled, the data read from Flash is decrypted automatically and returned to CPU.

- UKEY[63:0]: Stores keys for Flash encryption and decryption, which is set by users. If the values stored in address 0x1fff_f828 and 0x1fff_f82c is not 0xffff ffff, the return value is 0xaaaa_aaaa when reading these addresses.
- IWDG_RL_IV[11:0]: Stores the initial value of the IWDG_RLR register. If IWDG acts as a hardware watchdog, configure the IWDG_RL_IV register to set the interval of the IWDG reset time.
- IWDG_INI_KEY[31:0]：Determines whether IWDG_RL_IV is valid or not. When the value of IWDG_INI_KEY equals to 0xa5a5_5b1e, IWDG_RL_IV is valid, otherwise it is invalid.
- LSI_LP_CTL[31:0]：Entering the Stop mode after IWDG is enabled, the system can be woken up by IWDG via configuring LSI_LP_CTL.
  - If LSI_LP_CTL is set to 0x369c_f0f0, when MCU enters the Stop or Standby mode, LSI can be turned off according to the LSION value. After MCU is woken up, LSI recovers to the state before entering these modes.
  - If LSI_LP_CTL is not set, the system can be woken up by IWDG periodically after IWDG is enabled and MCU enters the Stop or Standby mode.
- DBG_CLK_CTL[15:0]: When DBG_CLK_CTL equals to 0x1234_bcde, CPU debug clock is turned off, otherwise it stays on.

3.2.3 SRAM

HK32F103xCxDxE integrates a 64 Kbytes SRAM. CPU can access SRAM fast with zero wait state to meet the requirements of most applications.

3.3 CRC Calculation Unit

CRC is used to verify data transmission or storage integrity. HK32F103xCxDxE integrates a CRC calculation unit to reduce application processing burden and accelerate processing.

CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time, and stored at a given memory location.

3.4 FSMC

- Supports external static memories, including SRAM, NOR Flash memory and PSRAM.
- Supports two NAND Flash interfaces and hardware ECC checks (data size up to 8 Kbytes).
- Supports a 16-bit PC card interface.
- Supports Burst access to synchronous devices (NOR Flash and PSRAM).
- 8-bit or 16-bit databus.
- Independent chip selection (CS) and configuration registers for each external memory.
- Programmable sequential control function for different devices:
  - Programmable wait states (up to 15)
  - Programmable bus turnaround cycles (up to 15)
  - Programmable read/write enable delays (up to 15)
  - Independent read/ write timings and protocol, to support as much different category memories and the timings
- Access continuous 32-bit address space of external 16-bit or 8-bit memories via 32-bit AHB transmission.
- Buffer of a data length is used to release the system bus when accessing an external low-speed memory for write operation.
- Asynchronous wait control logic for external memories.
- Supports write-encrypting and read-decrypting for 16-bit external memories.

- Supports Intel 8080 mode and Motorola 6800 mode, and can flexibly connect to various LCD controllers.

3.5 NVIC

HK32F103xCxDxE embeds a nested vectored interrupt controller (NVIC) to manage interrupt flexibly with the low interrupt latency.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector address passes directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processes late arriving higher-priority interrupts
- Supports tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

Table 3-3 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0X0000_0000
-	-3	Fixed	Reset	Reset	0X0000_0004
-	-2	Fixed	NMI	Non-maskable interrupt The RCC Clock Security System (CSS) is linked to the NMI vector.	0X0000_0008
-	-1	Fixed	HardFault	All class of fault	0X0000_000C
-	0	Settable	MemManage	Memory management	0X0000_0010
-	1	Settable	BusFault	Pre-fetch fault, memory access fault	0X0000_0014
-	2	Settable	UsageFault	Undefined instruction or illegal state	0X0000_0018
-	-	-	-	Reserved	0X0000_001C - 0X0000_002B
-	3	Settable	SVCall	System service call via SWI instruction	0X0000_002C
-	4	Settable	Debug Monitor	Debug Monitor	0X0000_0030
-	-	-	-	Reserved	0X0000_00034
-	5	Settable	PendSV	Pendable request for system service	0X0000_0038
-	6	Settable	SysTick	System tick timer	0X0000_003C
0	7	Settable	WWDG	Window watchdog interrupt	0X0000_0040
1	8	Settable	PVD	PVD through EXTI Line detection interrupt	0X0000_0044
2	9	Settable	TAMPER	Tamper interrupt	0X0000_0048
3	10	Settable	RTC	RTC global interrupt	0X0000_004C
4	11	Settable	FLASH	Flash global interrupt	0X0000_0050
5	12	Settable	RCC	RCC global interrupt	0X0000_0054
6	13	Settable	EXTI0	EXTI Line0 interrupt	0X0000_0058
7	14	Settable	EXTI1	EXTI Line1 interrupt	0X0000_005C
8	15	Settable	EXTI2	EXTI Line2 interrupt	0X0000_0060
9	16	Settable	EXTI3	EXTI Line3 interrupt	0X0000_0064
10	17	Settable	EXTI4	EXTI Line4 interrupt	0X0000_0068
11	18	Settable	DMA1_Channel1	DMA1 Channel1 global interrupt	0X0000_006C

Position	Priority		Name	Description	Address
12	19	Settable	DMA1_Channel2	DMA1 Channel2 global interrupt	0X0000_0070
13	20	Settable	DMA1_Channel3	DMA1 Channel3 global interrupt	0X0000_0074
14	21	Settable	DMA1_Channel4	DMA1 Channel4 global interrupt	0X0000_0078
15	22	Settable	DMA1_Channel5	DMA1 Channel5 global interrupt	0X0000_007C
16	23	Settable	DMA1_Channel6	DMA1 Channel6 global interrupt	0X0000_0080
17	24	Settable	DMA1_Channel7	DMA1 Channel7 global interrupt	0X0000_0084
18	25	Settable	ADC1_2	ADC1 and ADC2 global interrupt	0X0000_0088
19	26	Settable	USB_HP_CAN_TX	USB high priority or CAN TX interrupts	0X0000_008C
20	27	Settable	USB_LP_CAN_RX0	USB low priority or CAN RX0 interrupts	0X0000_0090
21	28	Settable	CAN_RX1	CAN RX1 interrupt	0X0000_0094
22	29	Settable	CAN_SCE	CAN SCE interrupt	0X0000_0098
23	30	Settable	EXTI9_5	EXTI Line[9:5] interrupts	0X0000_009C
24	31	Settable	TIM1_BRK_TIM9	TIM1 Break interrupt and TIM9 global interrupt	0X0000_00A0
25	32	Settable	TIM1_UP_TIM10	TIM1 Update interrupt and TIM10 global interrupt	0X0000_00A4
26	33	Settable	TIM1_TRG_COM_TIM11	TIM1 Trigger and Commutation interrupts and TIM11 global interrupt	0X0000_00A8
27	34	Settable	TIM1_CC	TIM1 Capture Compare interrupt	0X0000_00AC
28	35	Settable	TIM2	TIM2 global interrupt	0X0000_00B0
29	36	Settable	TIM3	TIM3 global interrupt	0X0000_00B4
30	37	Settable	TIM4	TIM4 global interrupt	0X0000_00B8
31	38	Settable	I2C1_EV	I2C1 event interrupt	0X0000_00BC
32	39	Settable	I2C1_ER	I2C1 error interrupt	0X0000_00C0
33	40	Settable	I2C2_EV	I2C2 event interrupt	0X0000_00C4
34	41	Settable	I2C2_ER	I2C2 error interrupt	0X0000_00C8
35	42	Settable	SPI1	SPI1 global interrupt	0X0000_00CC
36	43	Settable	SPI2	SPI2 global interrupt	0X0000_00D0
37	44	Settable	USART1	USART1 global interrupt	0X0000_00D4
38	45	Settable	USART2	USART2 global interrupt	0X0000_00D8
39	46	Settable	USART3	USART3 global interrupt	0X0000_00DC
40	47	Settable	EXTI15_10	EXTI Line[15:10] interrupts	0X0000_00E0
41	48	Settable	RTCAlarm	RTC alarm through EXTI line interrupt	0X0000_00E4
42	49	Settable	USBWakeUp	USB wakeup from suspend through EXTI line interrupt	0X0000_00E8
43	50	Settable	TIM8_BRK_TIM12	TIM8 Break interrupt and TIM12 global interrupt	0X0000_00EC
44	51	Settable	TIM8_UP_TIM13	TIM8 Update interrupt and TIM13 global interrupt	0X0000_00F0
45	52	Settable	TIM8_TRG_COM_TIM14	TIM8 Trigger and Commutation interrupts and TIM14 global interrupt	0X0000_00F4
46	53	Settable	TIM8_CC	TIM8 Capture Compare interrupt	0X0000_00F8
47	54	Settable	ADC3	ADC3 global interrupt	0X0000_00FC
48	55	Settable	FSMC	FSMC global interrupt	0X0000_0100

Position	Priority		Name	Description	Address
49	56	Settable	SDIO	SDIO global interrupt	0X0000_0104
50	57	Settable	TIM5	TIM5 global interrupt	0X0000_0108
51	58	Settable	SPI3	SPI3 global interrupt	0X0000_010C
52	59	Settable	USART4	USART4 global interrupt	0X0000_0110
53	60	Settable	USART5	USART5 global interrupt	0X0000_0114
54	61	Settable	TIM6	TIM6 global interrupt	0X0000_0118
55	62	Settable	TIM7	TIM7 global interrupt	0X0000_011C
56	63	Settable	DMA2_Channel1	DMA2 Channel1 global interrupt	0X0000_0120
57	64	Settable	DMA2_Channel2	DMA2 Channel2 global interrupt	0X0000_0124
58	65	Settable	DMA2_Channel3	DMA2 Channel3 global interrupt	0X0000_0128
59	66	Settable	DMA2_Channel4_5	DMA2 Channel4 and Channel5 global interrupts	0X0000_012C

3.6 EXTI

HK32F103xCxDxE embeds 16 external interrupt/event controller (EXTI) lines. EXTI0 to EXTI5 connects to IOs. The trigger event of each EXTI line can be configured and masked independently. The trigger event can be a rising edge, a falling edge or both.

3.7 Reset

HK32F103xCxDxE supports System reset, Backup domain reset and Power reset.

3.7.1 System reset

Except for the reset flags in the RCC_CSR register and registers in the backup domains, System reset signal resets all the registers.

When any of the following events occurs, System Reset signal is generated:

- Low-level voltage on NRST pin (External Reset)
- Window watchdog counting terminates (WWDG Reset)
- Independent watchdog counting terminates (IWDG Reset)
- Software reset (SW Reset)
- Low-power consumption management reset

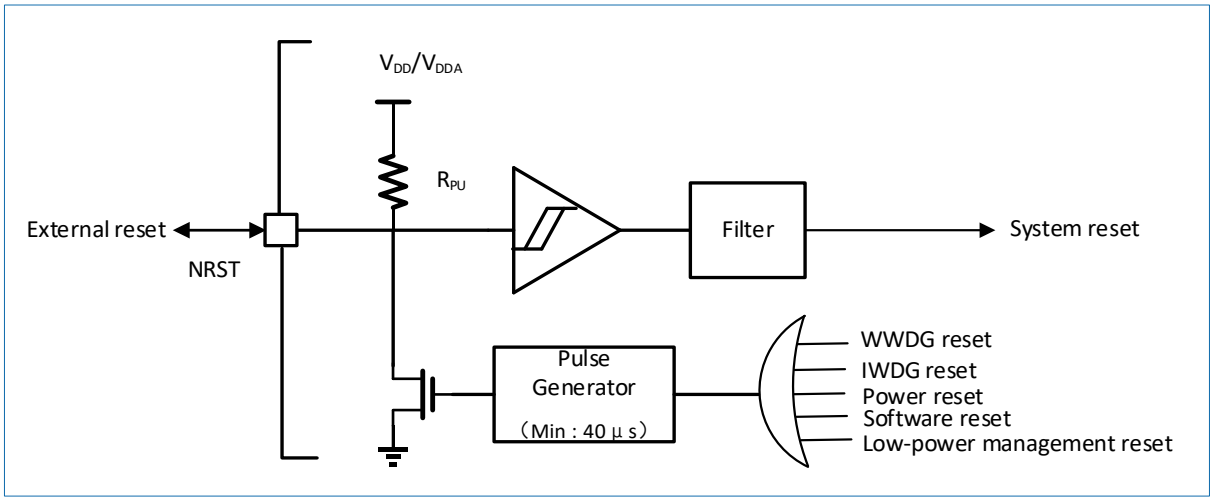

Figure 3-3 System reset

An Internal Reset signal is output via the NRST pin. A Pulse generator guarantees that each reset source produces at least 40 µs pulse latency. When NRST pin is pulled down and a reset pulse is generated for an external reset.

You can identify a reset source by checking reset state flags in the RCC_CSR register.

Table 3-4 Reset setting

Software reset	By setting the SYSRESETREQ bit to '1' or generating a Cortex-M3 interrupt to perform Software reset.
Low-power consumption management reset	To generate a low-power management reset when entering Standby mode: Set the nRST_STDBY bit in Option bytes to '1' to enable the low-power management reset function. Then, even it is in the process of entering Standby mode, the system will be reset instead of enter Standby mode.
	To generate a low-power management reset when entering Stop mode: Set the nRST_STDBY bit in Option bytes to '1' to enable the low-power management reset function. Then, even it is in the process of entering Stop mode, the system will be reset instead of enter Standby mode.

3.7.2 Power reset

Power reset signal resets all registers except for the registers in the backup domain. The reset source affects the reset pin, and keeps low level in the progress of reset. Reset entry vector is fixed on address 0x0000_0004.

When the following event occurs, Power reset signal is generated:

- POR/PDR reset
- Return from Standby mode

HK32F103xCxDxE embeds POR/PDR circuits. The circuits always operate to ensure the system runs well when power supply is over than POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, MCU resets and no external reset circuit is required.

3.7.3 Backup domain reset

Backup domain has two dedicated reset signals, which only affect the backup domain. When the following event occurs, backup domain reset signal is generated:

- Set BDRST bit in the RCC_BDCR register (trigger the software reset too).
- After both V_{DD} and V_{BAT} are powered down, power on V_{DD} and V_{BAT}.

3.8 Clock

HK32F103xCxDxE selects a system clock when it starts. When it resets, 8 MHz HSI RC is selected by default as system clock, and then 4-32 MHz external clock can be selected. When the external clock is disabled, it will be isolated and a corresponding interrupt is generated. More clock frequencies can be produced by using PLL.

HK32F103xCxDxE also provides LSI, LSE, GPIO input as clock source for the low-power and low-cost design scheme.

HK32F103xCxDxE integrates a clock security system (CSS) circuit. The detected HSE frequency threshold is adjustable.

3.8.1 Clock source

Table 3-5 clock sources

HSI oscillator	• Frequency: 56 MHz • Accuracy: full temperature range ± 2%
HSE oscillator	• 4-32 MHz oscillator

	• OSC_IN can be used as an external clock input (up to 64 MHz)
PLL clock	• Input frequency: 2-56 MHz • Output frequency: 30-120 MHz
LSI clock	Frequency: 30-60 kHz (typical: 40 kHz)
LSE clock	• Frequency: 32.768 kHz • OSC32_IN can be used as external clock input (32.768 kHz)
GPIO input clock	PA1, PB1, PC7, PB7 (up to 64 MHz)

3.8.2 Clock tree

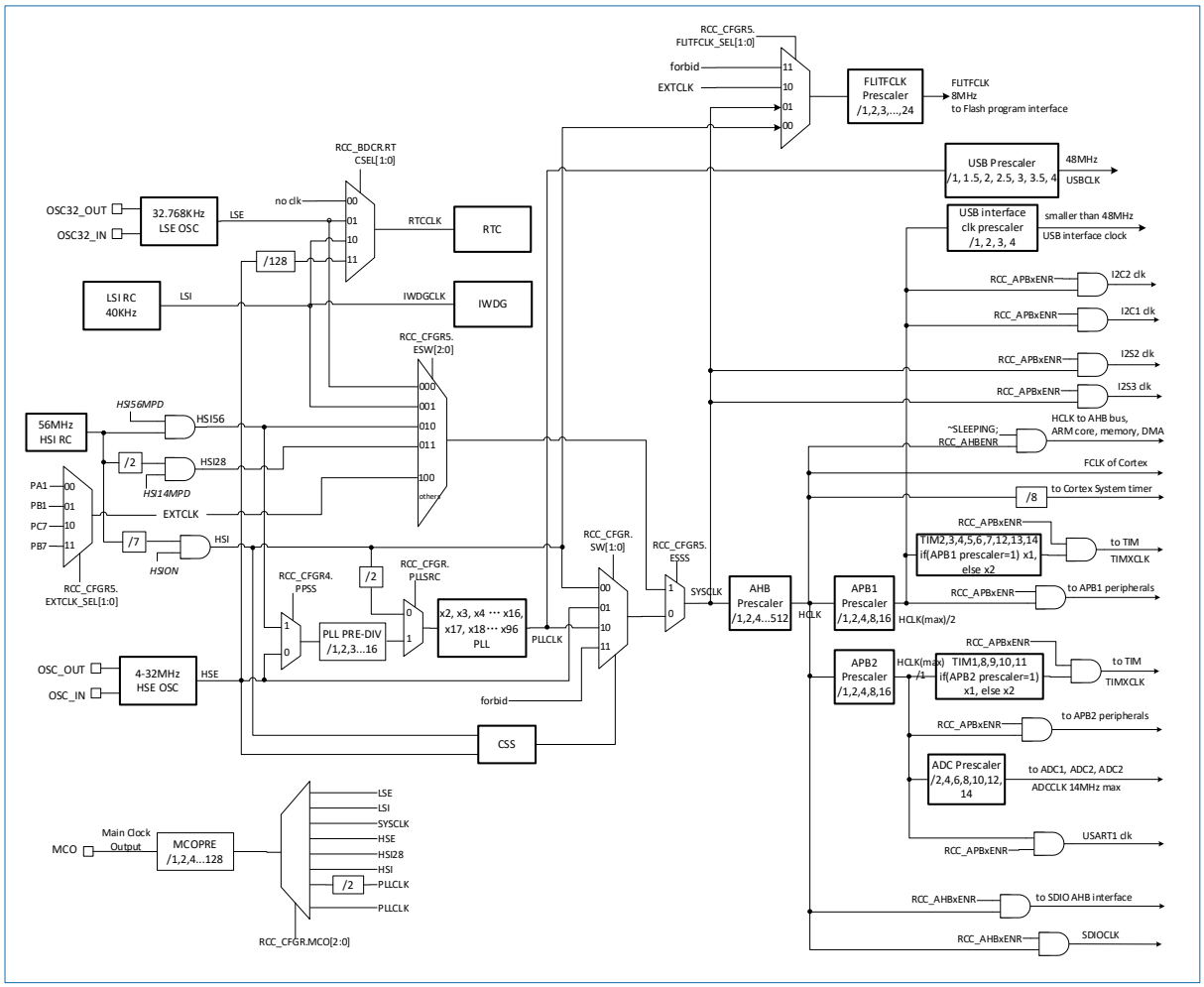

Figure 3-4 clock tree

- PLL：chosen from HSI8M/2, HSI56M/PREDIV or HSE/PREDIV.
- SYSCLK：chosen from HSI8M, HSI28M, HSI56M, HSE, PLL, LSI, LSE or GPIO input clock. HSI8M is the default clock.
- FLITFCLK：chosen from HSI8M, GPIO input clock or SYSCLK clock.

3.9 Boot mode

When the system starts, the Boot pin is used to select one mode from three modes:

- Boot from Flash block
- Boot from the system memory

- Boot from the internal SRAM

Bootloader program is stored in the system memory. It can reprogram Flash via the USART1 interface.

3.10 Power Supply schemes

HK32F103xCxDxE adopts a single power supply, V_{DD} and V_{DDA} multiplex the same pin to supply power for digital and analog circuits. V_{DD} and V_{DDA} is in the range of 1.8 to 3.6 V.

- V_{DD}: 1.8V - 3.6V

V_{DD} pin supplies power for I/O pins and internal LDOs.

- V_{DDA}: 1.8V - 3.6V

V_{DDA} pin supplies power for the analog circuitry, such as ADC and the temperature sensor.

- V_{BAT}: 1.8V - 3.6V

When V_{DD} is powered down, the internal power switch circuit supplies power for RTC, the external 32.768 kHz oscillator and backup registers via V_{BAT}.

3.11 PVD

HK32F103xCxDxE integrates a programmable voltage detector (PVD). The PVD monitors V_{DD} power supply and compare it to the V_{PVD} threshold. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated. The interrupt program sends a warning message and/or switches MCU into Safe mode. The PVD is enabled by software.

3.12 Low-power modes

HK32F103xCxDxE supports several low-power modes to achieve the best compromise between low power consumption, short startup time and available wake-up sources.

- Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

In Stop mode, MCU achieves the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all internal clocks, the PLL, the HSE oscillators and the HSI oscillators are disabled. MCU can be woken up from Stop mode by any EXTI line. The EXTI line source can be any one of external I/O pins, a PVD output, or a RTC alarm signal.

- Standby mode

In Standby mode, MCU achieves the lowest power consumption. The internal LDO is off, so the entire 1.2V domain is powered off. The PLL, the HSE oscillators and the HSI oscillators are disabled. In Standby mode, the content in SRAM and registers are lost except for the ones of registers in the backup domain and Standby circuitry.

MCU exits from Standby mode when an external reset (NRST), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

For more information of power consumption of different modes, pls see Table 4-7.

The conditions of entering and exiting low-power modes as following:

Table 3-6 conditions of entering and exiting low-power modes

Operation mode	Entering the low-power mode	Wake-up condition
Sleep mode	To set: 1. PWR_CR: LPDS = 0. 2. PWR_CR: PDDS =0. 3. Perform WFI/WFE command by software.	Any IRQ interrupt/event, including System tick timer.

Operation mode	Entering the low-power mode	Wake-up condition
Stop mode	To set: 1. PWR_CR: PDDS = 1. 2. Set the SLEEPDEEP bit in the Cortex-M3 system control register. 3. Perform WFI/WFE command by software.	● Any EXTI line ● MCU is pre-woken up by ADC sampling. Really wake-up occurs when the conditions are met. ● DAC outputs hold
Standby mode	To set: 1. PWR_CR: LPDS = 0. 2. PWR_CR: PDDS =1. 3. Set the SLEEPDEEP bit in the Cortex-M3 system control register. 4. Perform WFI/WFE command by software.	● 3 polarity-configurable external pins and an RTC alarm can wake up the system. ● Supports DAC output maintenance.

3.13 DMA

The flexible general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) manage the transfers from memories to memories, devices to memories, and memories to devices. The two DMAs supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel has a dedicated hardware DMA request logic, and can also be triggered by software. Transferring sizes, source address and destination address can be set independently by software. DMA can be used with the main peripherals, such as SPI, I2C, USART, general-purpose, basic and advanced-control timers, SDIO and ADC.

3.14 RTC and BKP

RTC and the backup registers use a switch to control power supply. When V_{DD} is enabled, it is switched to V_{DD} to supply power, otherwise it is switched to the V_{BAT} pin.

Real-time clock provides a set of continuously running counters which can be used with software to provide a clock calendar, and provides an alarm interrupt and a periodic interrupt.

3.14.1 RTC

The driven clock of RTC can be a 32.768 kHz external oscillator or an internal low-power RC oscillator. The typical frequency of the internal RC oscillator is 40 kHz. To compensate any natural quartz deviation, the RTC can be calibrated by an external 512 Hz output. The RTC has a 32-bit programmable counter for long term measurement by using the Compare register to generate an alarm. A 20-bit pre-scaler is used for the time clock and is configured by default to generate a time base of 1 second from a clock at 32.768 kHz.

3.14.2 BKP

Backup registers are used to store user application data. The system reset and power reset do not reset these registers. When woken up from Standby mode, these registers are not reset. HK32F103xCxDxE has the BKP_DR0 to BKP_DR10 registers in backup domain.

3.15 Independent Watchdog

The Independent watchdog (IWDG) is based on a 12-bit down counter and an 8-bit pre-scaler. The IWDG is clocked from an internal independent 40 kHz RC. Because the RC is independent from the main clock, the IWDG can operate in Stop mode and Standby mode. It can work as a watchdog to reset the system when a problem occurs, or as a free running timer for application timeout management. IWDG can be configured to a software or hardware watchdog through Option bytes. In debug mode, the counter can be frozen.

IWDG supports the watchdog window mode (by set the IWDG_WINR register). The original reset value of IWDG timer is set by Flash option bytes.

3.16 Window Watchdog

Window watchdog (WWDG) is based on a 7-bit down counter. The counter can be set to the free running mode or used as a watchdog to reset the system when a problem occurs. It is clocked from the main clock and has an early warning interrupt capability. In debug mode, the counter can be frozen.

3.17 SysTick Timer

SysTick timer is dedicated to the operation system as a standard down counter. Its features:

- 24-bit down counter
- Auto-reload capability
- Generate a maskable interrupt when the counter reaches 0.
- Programmable clock source

3.18 Basic Timer

HK32F103xCxDxE integrates two basic timers (TIM6 and TIM7).

Basic timer can be used as a general-purpose time base timer. Basic timer is used to generate a CPU interrupt request at fixed time.

3.19 General-purpose Timer

Every general-purpose timer (TIM2/TIM3/TIM4/TIM5) provides a 16-bit auto-reload up/down counter, a 16-bit pre-scaler and 4 independent channels. Every channel can be used for input capture, output compare, PWM and a single pulse output. Up to 16 input captures, output compares, PWM channels are provided in the maximum package.

General-purpose timers can corporate with advanced timers through Timer Linking feature for synchronization and event chaining. In debug mode, the counter can be frozen. Every general-purpose timer supports an independent DMA request mechanism.

TIM2, TIM3, TIM4 and TIM5 support the following features:

- CCER[15]: CC4NP field in the CCER register for input rising and falling edges triggering
- CCER[11]: CC3NP field in the CCER register for input rising and falling edges triggering
- CCER[7]: CC2NP field in the CCER register for input rising and falling edges triggering
- CCER[3]: CC1NP field in the CCER register for input rising and falling edges triggering
- 4 channels support falling edge, and rising and falling edges triggering.

3.20 Advanced Timer

HK32F103xCxDxE integrates an advanced timer (TIM1/TIM8).

The advanced timer can be seen as a three-phase PWM generator multiplexed on 6 channels, and used as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output
- Complementary PWM outputs with programmable inserted dead-times

If configured as a standard 16-bit timer, an advanced timer has the same functions as the general-purpose timer. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%). Because most of its internal structure is the same as that of a general-purpose timer. The advanced timer can work together with general-

purpose timers via Timer Link feature for synchronization or event chaining. In debug mode, the counter can be frozen.

The advanced timers provide DAC trigger and the following functions:

- CCER[15]: CC4NP field in the CCER register for input rising and falling edges triggering
- CR1[15]: ETR_CLR_SEL field in the CR1 register for clearing PWM outputs through an external pin or voltage comparator VC4.
- CR1[14]: BRK_SEL field in the CR1 register for selecting an external pin or voltage comparator VC1/VC2/VC3 to output PWM break.
- 4 channels support falling edge, and rising and falling edges triggering.

3.21 I2C bus

Two I2C bus interfaces can work as a master or a slave and support standard and fast mode. The I2C interface supports 7-bit or 10-bit addressing mode. It supports double-slave address addressing in 7-bit slave mode. The I2C interface embeds a hardware CRC generator/verification. They can be served by DMA and they support SMBus V2.0/PMBus.

3.22 USART

HK32F103xCxDxE embeds five universal synchronous/asynchronous receiver transmitters (USART1/USART 2/USART3/USART4/USART5). These interfaces provide asynchronous communications, IrDA SIR ENDEC su pport, multi-processor communications, single-wire half-duplex communications and have LIN Master/Sl ave capability.

The USART1 is able to communicate at speeds of up to 4.5Mbit/s. The other interfaces communicated at speed up to 2.25 Mbit/s.

All the USART interfaces provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant), and SPI-like communications capability.

Table 3-7 USART features

Features	USART1/USART2/USART3/USART4/USART5
Hardware flow control	Yes
DMA continuous transmission	Yes
Multi-processor communications	Yes
Synchronous mode	Yes
Smart Card mode	Yes
Single-wire half-duplex communications	Yes
IrDA SIR ENDEC	Yes
LIN Master/Slave mode	Yes
Dual clock domain and wake up from Stop mode	Yes
Receiver timeout interrupt	Yes
ModBus communications	Yes

3.23 SPI

HK32F103xCxDxE has three SPI interfaces. In master or slave mode, full-duplex and half-duplex communicate speed is up to 18 Mbit/s. The 3-bit pre-scaler gives 8 master mode frequencies. Each frame can be configured to 8 or 16 bits. The hardware CRC generation/verification supports basic SD card and MMC mode.

All SPIs can be served by the DMA controller.

The three SPI interfaces can operate in I2S mode. The standard I2S interfaces can run in master or slave mode. The three interfaces can be configured to 16/32 bits transmission, or input/output channels. They support audio sampling from 8 kHz to 48 kHz. When one I2S interface is configured as a master, its main clock can output 256 times sampling frequency to an external DAC or CODEC.

Table 3-8 SPI features

Features	SPI1/SPI2/SPI3
Hardware CRC computation	Yes
RX/TX buffer	Yes
NSS pules mode	Yes
I2S mode	Yes
TI mode	Yes

3.24 SDIO

An SD/SDIO/MMC host interface supports Multi-Media-Card (MMC) System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48MHz, and is compliant with SD Memory Card Specification Version 2.0.

SDIO Card Specification Version 2.0 supports two databus modes: 1-bit (default) and 4-bit. The current version supports only one SD/SDIO/MMC4.2 card each time but a stack of MMC4.1 or previous versions each time. In addition to SD/SDIO/MMC, the interface is compatible with the CE-ATA digital protocol version 1.1.

3.25 CAN

HK32F103xCxDxE has an independent CAN interface. The CAN interface is compliant with Specification 2.0A and 2.0B (active). Its bit speed rate is up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has 3 transmit mailboxes and 2 receive FIFOs with 3 stages 14 scalable filter banks.

3.26 USB

HK32F103xCxDxE embeds a USB device peripheral compatible with USB full-speed. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz for USB is generated by the internal main PLL.

3.27 GPIO

Each GPIO pin can be configured by software as output (push- pull or open-drain), input (with or without pull-up or pull-down) or peripheral alternate functional. Most of GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable. The I/Os alternate function configuration can be locked in order to avoid spurious writing to the I/O registers.

3.28 ADC

HK32F103xCxDxE embeds 3 12-bit ADCs. Every ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, the conversion on the specified analog input channel executes automatically.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single sample

The ADC can be served by DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. When the monitored signal is over the preset threshold, an interrupt is generated. The events generated by general-purpose/advanced timers can connect to the ADC start/ injection trigger event respectively. The application program then synchronizes A/D conversion and timer.

In Stop mode, RTC times and sends a signal to ADC; ADC samples the signal and then wakes up the ADC clock. The ADC clock gets ready, and then triggers ADC conversions and generates an AWD event according to ADC conversion results. Then, the AWD event is sent to an EXTI line to wake up the system.

3.29 DAC

HK32F103xCxDxE integrates two 12-bit DACs with buffer. They are used to convert 2-channel digital signals to 2-channel analog voltage signals and output them. This function is realized by integrated resistor strings and an amplifier in inverting configuration.

The two digital interface supports the following features:

- Two DAC converters, with an output channel for each
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Input reference voltage V_{REF+}

HK32F103xCxDxE has eight ADC trigger inputs. The update outputs of timers can trigger the DAC channel, and connect to the different DMA channels.

3.30 Temperature sensor

Temperature sensor generates a voltage that varies linearly to temperature. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into digital value.

3.31 96-bit UID

A 96-bit unique identification (UID) provides a reference number corresponding to each HK32F103xCxDxE SOC. Under any circumstance, the UID is unique. You are prohibited to modify the UID. Depends on different applications, the 96-bit UID can be read in unit of byte (8 bits), half-word (16 bits) or word (32 bits). The 96-bit UID is suitable for the following applications:

- As a part number (for example, as a USB character serial number or other terminal applications).
- As a keyword. When programming the Flash, use the UID together with software encryption and decryption algorithm to enhance security of the code in the Flash.
- Activating the boot process of the security mechanism.

3.32 Debug Interface

Build-in ARM SWJ-DP interface is combined with a single wire debug interface. It can build connection between serial single wire debug interfaces (SWDIO and SWCLK). The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK. A specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

The ARM® Embedded Trace Macrocell (ETM) provides a greater visibility of the instruction and data flow inside

the CPU core by streaming compressed data at a high rate from HK32F103xCxDxE through a number of ETM pins to an external trace port analyzer (TPA) device. The TPA connects to a debug host via USB or other high-speed channels. The TPA connects to a debug host via USB or other high-speed channels.

A debugger software running on the debug host can record real-time instructions and data flow, and display them in the required format. TPA devices are available from development tool vendors and compatible with third party debugger software tools.

4 Electrical characteristics

4.1 Absolute maximum values

Note：

- *Stresses above the absolute maximum rating listed in Table 4-1 and Table 4-20 may cause permanent damage to the device.*
- *Exposure to maximum permitted conditions for extended periods may affect device reliability.*

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.5	4.0	V
V_{IN}	Input voltage on pins	V_{SS} - 0.3	V_{DD} + 4.0	
$\|\Delta V_{DDx}\|$	Variation between different V_{DD} Power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variation between different V_{DD} ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) (1)	150	mA
I_{VSS}	Total current out of Vss ground lines (sink) (1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$I_{INJ(PIN)}$ (2)	Injected current on pins (3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pin) (4)	±25	

(1). All main power (V_{DD}, V_{DDA}) and Ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

(2). Negative injected current disturbs the analog performance of the device.

(3). When $V_{IN} > V_{DD}$, a positive injected current is induced. When $V_{IN} < V_{SS}$, a negative injected current is induced, and the injected current must be limited to the permitted range.

(4). When several I/Os are submitted to a current injection, the maximum $\sum_{IINJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.1.3 Thermal characteristics

Table 4-3 Thermal characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–45 ~ +150	°C
T_J	Maximum junction temperature	125	

4.2 Operation conditions

4.2.1 General operation conditions

Table 4-4 General operation conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	60	
f_{PCLK2}	Internal APB2 clock frequency	0	120	
V_{DD}	Standard operating voltage	2	3.6	V
V_{DDA}	Analog operating voltage (1)	2	3.6	V
V_{BAT}	Backup operating voltage	1.8	3.6	V
T	operating temperature	-40	105	℃

(1). All main power (V_{DD} and V_{DDA}) pins must always be connected to the external power supply. It is recommended to add a filter capacitor.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0]=000	2.183	2.188	2.196	V
		PLS[2:0]=001	2.286	2.289	2.298	
		PLS[2:0]=010	2.393	2.399	2.407	
		PLS[2:0]=011	2.502	2.508	2.518	
		PLS[2:0]=100	2.621	2.629	2.639	
		PLS[2:0]=101	2.726	2.733	2.745	
		PLS[2:0]=110	2.839	2.846	2.855	
		PLS[2:0]=111	2.958	2.969	2.979	
	Programmable voltage detector level selection (falling edge)	PLS[2:0]=000	2.116	2.119	2.125	
		PLS[2:0]=001	2.208	2.211	2.220	
		PLS[2:0]=010	2.305	2.310	2.320	
		PLS[2:0]=011	2.399	2.406	2.416	
		PLS[2:0]=100	2.506	2.512	2.521	
		PLS[2:0]=101	2.596	2.602	2.613	
		PLS[2:0]=110	2.693	2.701	2.710	
		PLS[2:0]=111	2.798	2.805	2.817	

4.2.3 Embedded reference voltage

Table 4-6 Embedded reference voltage

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 ~ 105°C	0.74	0.8	0.811	V

4.2.4 Operating current

Table 4-7 Operating current characteristics

Mode	Conditions	V_{DD} = 3.3V				Unit
		-40° C	25° C	85° C	105° C	
Run Mode	HCLK=120MHz, 4 wait period for Flash read operation, APB clock is enabled (cache enable).	12.18	20.95	22.31	23.44	mA
	HCLK=120MHz, 4 wait period for Flash read operation, APB clock is disabled (cache enable).	6.71	11.50	12.74	13.81	mA
	HCLK = HSE(8MHz), 0 wait period for Flash read operation, APB clock is enabled (cache enable).	1.83	1.98	3.08	4.1	mA
	HCLK = HSE(8MHz), 0 wait period for Flash read operation, APB clock is disabled (cache enable).	1.19	1.36	2.39	3.41	mA
	HCLK = LSI(40 kHz)	0.23	0.31	1.34	2.33	mA
	HCLK =LSE(32.768 kHz)	0.23	0.3	1.35	2.32	mA
Sleep Mode	HCLK = 120 MHz, APB clock is enabled	8.52	14.63	15.92	17.01	mA
	HCLK = 120 MHz, APB clock is disabled.	3.3	5.65	6.82	7.85	mA
	HCLK = HSI (8 MHz), APB clock is enabled.	1.56	1.69	2.95	3.72	mA
	HCLK = HSI (8 MHz), APB clock is disable.	0.88	1.01	2.85	3.04	mA
Stop Mode	LDO operates at full speed, HSE/HSI/LSE is disabled, IWDG is disabled.	202.67	303	1322	2179	µA
	LDO low-power state, HSE/HSI/LSE is disabled, IWDG is disabled.	18.38	89.47	729	1374	µA
Standby Mode	LSI and IWDG are enabled.	2.98	3.87	16.74	30.29	µA
	LSI and IWDG are disabled.	2.96	3.87	16.68	30.22	µA
	All oscillators are disabled.	2.35	3.36	16.16	29.72	µA
Shutdown	LSE is enabled and RTC runs (BKPPDS = 0).	1.7	2.67	11.98	21.87	µA

Mode	Conditions	V_{DD} = 3.3V				Unit
		-40° C	25° C	85° C	105° C	
Mode	LSE and RTC are disabled (BKPPDS = 1).	0.04	0.09	0.62	1.60	μA
	LSE is disabled and RTC stops (BKPPDS = 0).	1.31	2.19	11.41	21.27	μA
V_{BAT}	LSE/LSI is enabled and RTC runs.	1.7	2.67	11.98	25.86	μA
	LSE/LSI is enabled and RTC stops.	1.31	2.19	11.41	21.27	μA

4.2.5 HSE clock characteristics

HK32F103xCxDxE integrates a HSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

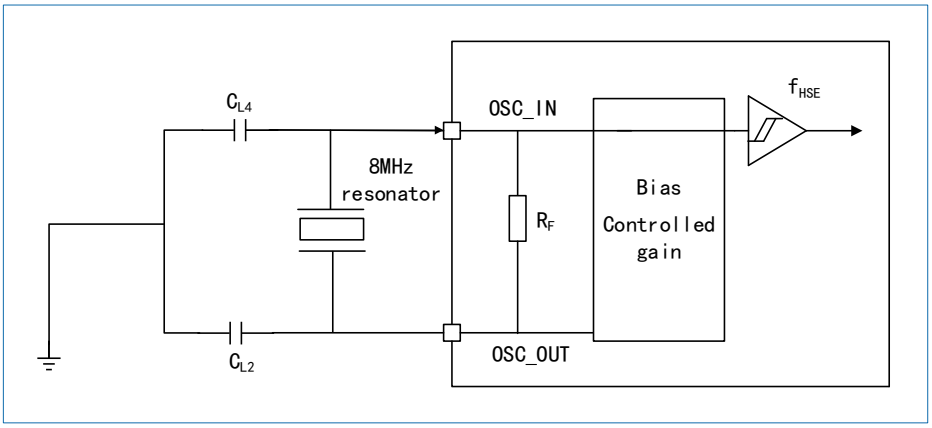

Figure 4-1 Typical application with HSE (8MHz)

HK32F103xCxDxE can be clocked from the OSC_IN pin. The requirements of this clock signal are described as follows:

Table 4-9 HSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	1	8	25	MHz
V_{HSEH}	OSN_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSN_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$T_{w(HSE)}$	OSN_IN high or low time		5	-	-	ns
$T_{r(HSE)}$/ $T_{f(HSE)}$	OSN_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSN_IN input capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

4.2.6 LSE clock characteristics

HK32F103xCxDxE integrates a LSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

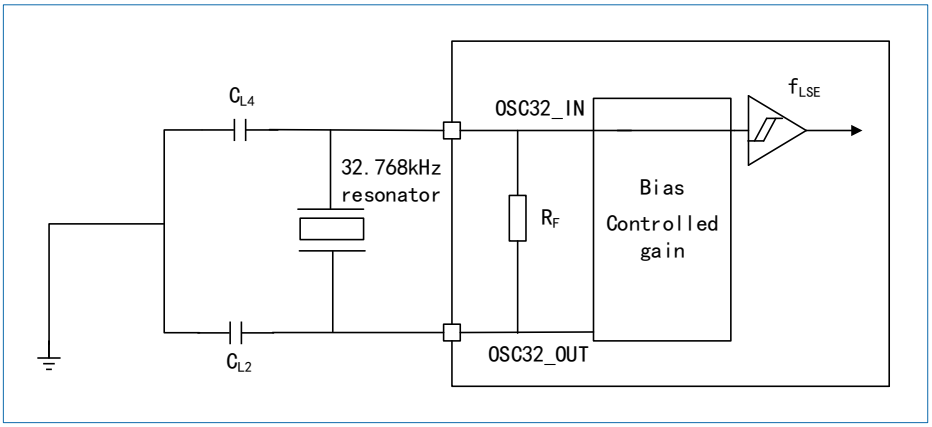

Figure 4-2 Typical application with LSE

HK32F103xCxDxE can be clocked from the OSC32_IN pin. The requirements of this clock signal are described as follows:

Table 4-10 LSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{LSE_ext}	External clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSN32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSN32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$T_{w(LSE)}$	OSN32_IN high or low time		450	-	-	ns
$T_{r(LSE)}$/ $T_{f(LSE)}$	OSN32_IN rise or fall time		-	-	50	
$C_{in(LSE)}$	OSN32_IN input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%

4.2.7 High-speed internal (HSI) RC oscillator

Table 4-8 HSI RC oscillator characteristics

Symbol	Description	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
$ACC_{(HSI)}$	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register		-	-	1	
		Factory calibrated	TA= –40 ~ +105°C	-2	-	2.5	%
			TA= –40 ~ +85°C	-1.5	-	2.2	%
			TA= 0~ +70°C	-1.3	-	2	%
			TA= 25°C	-1.1	-	1.8	%
$Tsu_{(HSI)}$	HSI oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		1	-	2	µs
$IDD_{(HSI)}$	HSI oscillator power consumption	-		-	80	100	µA

4.2.8 Low-speed internal (LSI) RC oscillator

Table 4-9 LSI RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	30	40	60	kHz

Symbol	Description	Conditions	Min	Typ	Max	Unit
$DuCy_{(LSI)}$	Duty cycle	-	40	50	60	%
$ACC_{(LSI)}$	Accuracy of the LSI oscillator	Factory setting: T_A= –40 ~+105 °C	-10	-	+10	%
$T_{su(LSI)}$	LSI oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	85	µs

4.2.9 PLL characteristics

Table 4-10 PLL characteristics

Symbol	Description	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL Input clock	1	8.0	25	MHz
	PLL input clock duty	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	120	MHz
t_{LOCK}	PLL Lock time	-	-	200	us
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.10 GPIO input clock

HK32F103xCxDxE is clocked form PA1, PB1, PC7, PB7 input clock.

Table 4-11 GPIO input clock characteristics

Symbol	Description	Value			Unit
		Min	Typ	Max	
F_{ext}	Input clock frequency	1	8.0	64	MHz
	Input clock duty	40	-	60	%
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.11 Flash memory characteristics

Table 4-12 Flash memory characteristics

Symbol	Description	Min	Typ	Max	Unit
T_{PROG}	A byte programming time	6	-	7.5	µs
T_{ERASE}	Page erase time	4	-	5	ms
	Mass erase time	30	-	40	ms
I_{DDPROG}	A byte programming current	-	-	5	mA
$I_{DDERASE}$	Page/mass erase current	-	-	2	mA
I_{DDREAD}	Supply current@24MHz (read mode)	-	2	3	mA
	Supply current@1MHz (read mode)	-	0.25	0.4	mA
N_{END}	Endurance	100	-	-	kcycles
t_{RET}	Data retention	20	-	-	year

4.2.12 I/O port characteristics

Table 4-13 I/O static characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	VDD = 3.3 V	1.6			V

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.5	V
V_{hys}	Schmitt trigger voltage hysteresis		450mV@3.3V	-	-	mV
I_{lkg}	Input leakage current	V_{IN} = 3.3 V	-	-	3	μA
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	30	40	50	KΩ
R_{PD}	Weak pull-down equivalent resistor	$V_{IN} = V_{DD}$	30	40	50	KΩ
C_{IO}	I/O pin capacitance		-	5	-	pF

4.2.13 Output voltage characteristics

Table 4-14 Output voltage characteristics

Speed mode	Symbol	Description	Conditions	Min	Max	Unit
10	V_{OL}	Output low level voltage	C_L = 50 pF, V_{DD} = 1.8 V ~ 3.6V R_{Load} = 5 Kohm	-	2	MHz
	V_{OH}	Output high level voltage		-	125	ns
01	V_{OL}	Output low level voltage	C_L = 50pF, V_{DD} = 1.8V ~ 3.6V R_{Load} = 5 Kohm	-	2	MHz
	V_{OH}	Output high level voltage		-	125	ns
11	V_{OL}	Output low level voltage	C_L = 50 pF, V_{DD} = 1.8V ~ 3.6V R_{Load} = 5 Kohm	-	2	MHz
	V_{OH}	Output high level voltage		-	125	ns

Table 4-15 Output voltage AC characteristics

Mode	Symbol	Description	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Max frequency	CL = 50 pF, VDD = 1.8 V ~ 3.6V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Max frequency	CL = 50 pF, VDD = 1.8 V ~ 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Max frequency	CL = 50 pF, VDD = 2.7 V ~ 3.6 V	-	50	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	5	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	5	ns

4.2.14 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit might connect to an external RC circuit or no circuit.

Table 4-16 NRST pin characteristics

Symbol	Description	Min	Max	Unit
V_{IL}	NRST input low level voltage	-	0.8	V

Symbol	Description	Min	Max	Unit
V_{IH}	NRST input high level voltage	2	-	V
V_{hys}	Schmitt trigger voltage hysteresis	-	200	mV
R_{pull}	Weak pull-up equivalent resistor	-	50	K
T_{Noise}	Low level is neglected	-	100	ns

4.2.15 TIM timer characteristics

Table 4-17 TIM characteristics

Symbol	Description	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIM\ x\ CLK}$
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$F_{TIMxCLK}/2$ (1)	MHz
Res $_{TIM}$	Timer resolution	-	16	bit
Tcounter	16-bit counter clock period when selecting an internal clock	1	65536	$T_{TIM\ x\ CLK}$
T_{MAX_COUNT}	Maximum possible count	-	65536x65536	$T_{TIM\ x\ CLK}$

(1). $f_{TIM\ x\ CLK}$ = 120 MHz

4.2.16 ADC characteristics

Table 4-18 ADC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	ADC power supply	-	2	3.3	3.6	V
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling frequency	-	0.05		1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-		17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	-	5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	8.3			$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3	$1/f_{ADC}$
t_S	Sampling rate	f_{ADC} = 14 MHz	0.107		17.1	µs
		-	1.5		239.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	0	0	1	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (ts for sampling +12.5 for successive approximation)			$1/f_{ADC}$
ADC bit width	12-bit (8 bits in valid)	-	-			-

4.2.17 DAC characteristics

Table 4-19 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	1.8	3.3	3.6	V
V_{REF+}	Reference supply voltage	1.8	3.3	3.6	V
V_{SSA}	Ground	0	0	0	V
R_{LOAD}	Resistive load with buffer ON	5	-	-	kΩ
R_O	Impedance output with buffer OFF	-	15	-	kΩ
C_{LOAD}	Capacitive load	-	-	-	pF
DAC_OUT min	Lower DAC_OUT voltage with buffer ON	0.1	-	-	V
DAC_OUT max	Higher DAC_OUT voltage with buffer ON			V_{DD}-0.1	V
DAC_OUT min	Lower DAC_OUT voltage with buffer OFF	0	-	-	mV
DAC_OUT max	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF}	V
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	108	135	162	μA
I_{DDA}	DAC DC current consumption in quiescent mode	-	-	429	μA
		-	-	429	μA
DNL	Differential non linearity Difference between two consecutive code-1LSB	-	-	±1	LSB
				±1	LSB
INL	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)			±4	LSB
				±4	LSB
Offset	Offset error (difference between measured value at Code (0x800) and the ideal value = VREF+/2)			±10	mV
				±12	LSB
Gain error	Gain error			±0.5	%
$t_{SETTLING}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB		3	4	μs
Update rate (3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)			1	MSPS
t_{WAKEUP}	Wakeup time from off state (Setting the ENx bit in the DAC Control register)		6.5	10	μs
PSRR+	Power supply rejection ratio (to VDDA) (static DC measurement)		67	40	dB

4.2.18 Temperature sensor characteristics

Table 4-20 Temperature sensor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Sensor gain	-	2.9	3	3.1	mV/℃

5 Typical circuitry

5.1 Power supply scheme

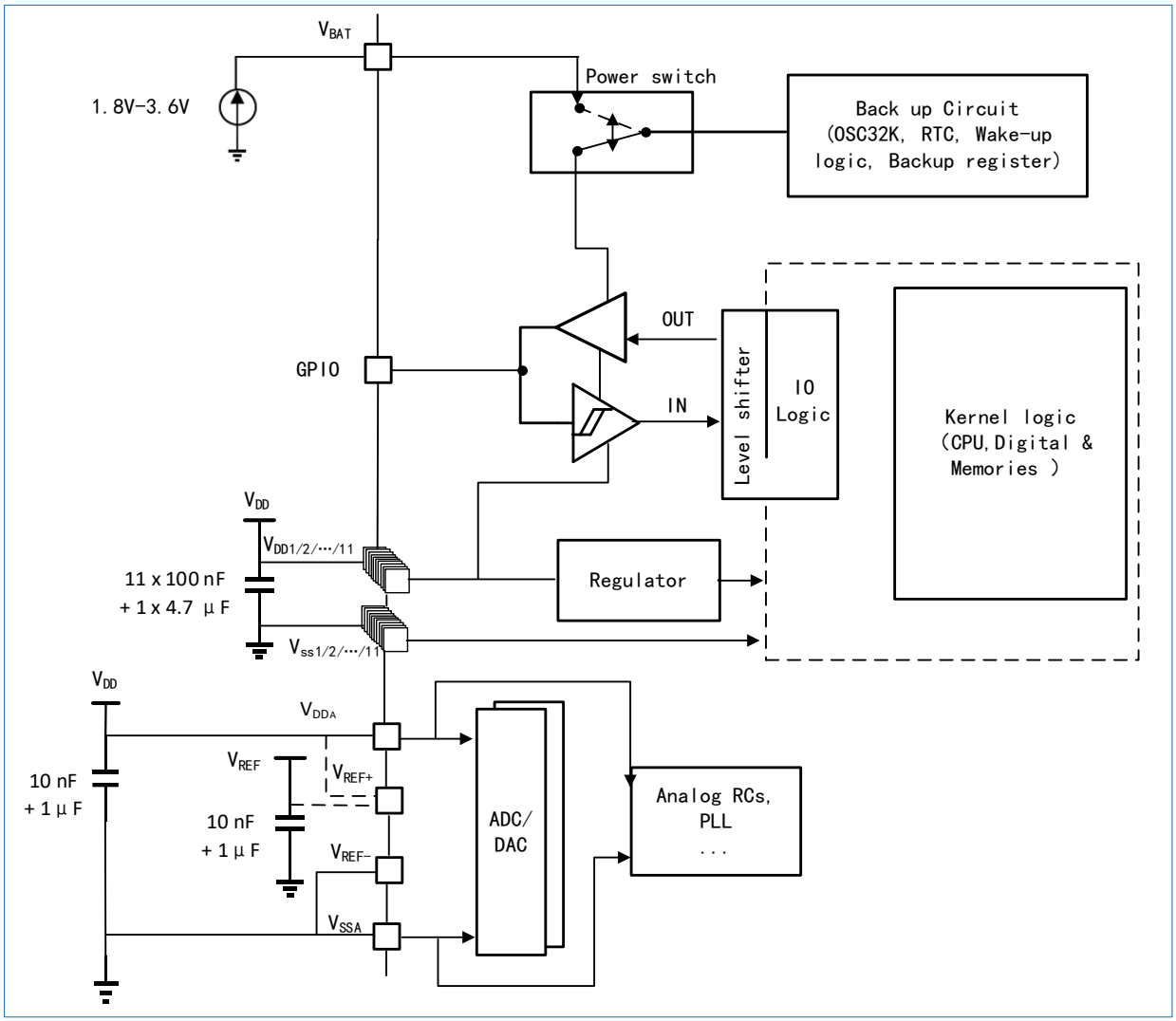

Figure 5-1 Power Supply scheme

6 Pinouts and pin descriptions

HK32F103xCxDxE is available in two packages: LQFP64/LQFP100.

6.1 LQFP64

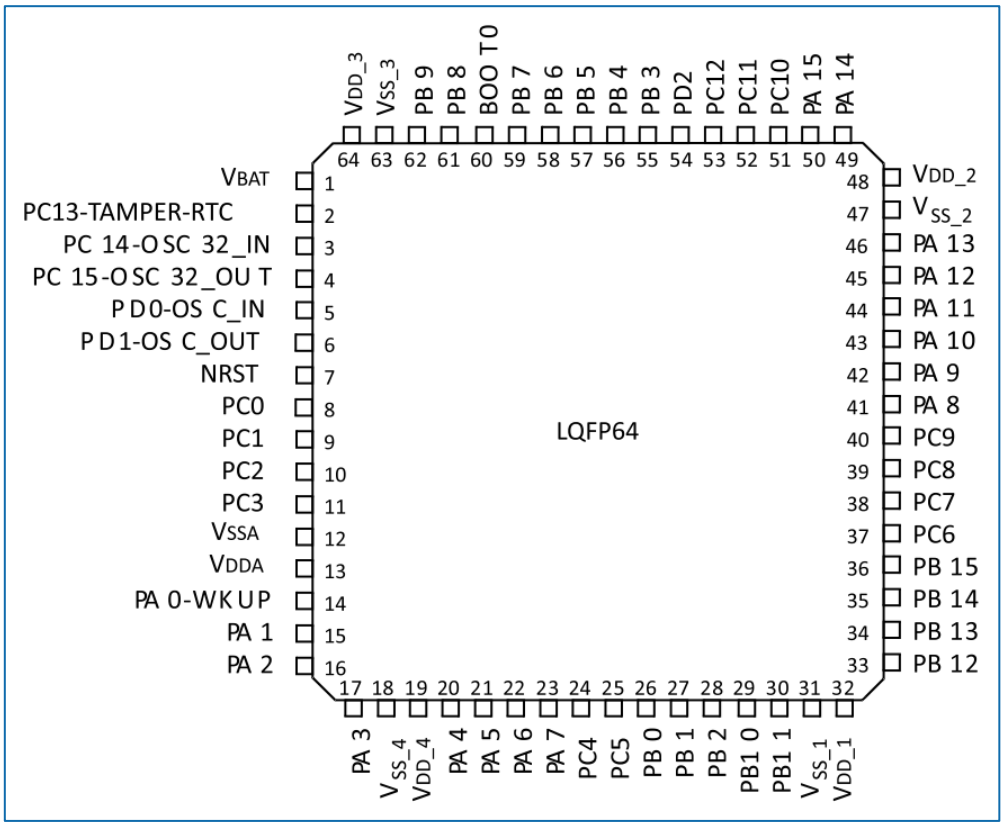

Figure 6-1 LQFP64 package pinout

6.2 LQFP100

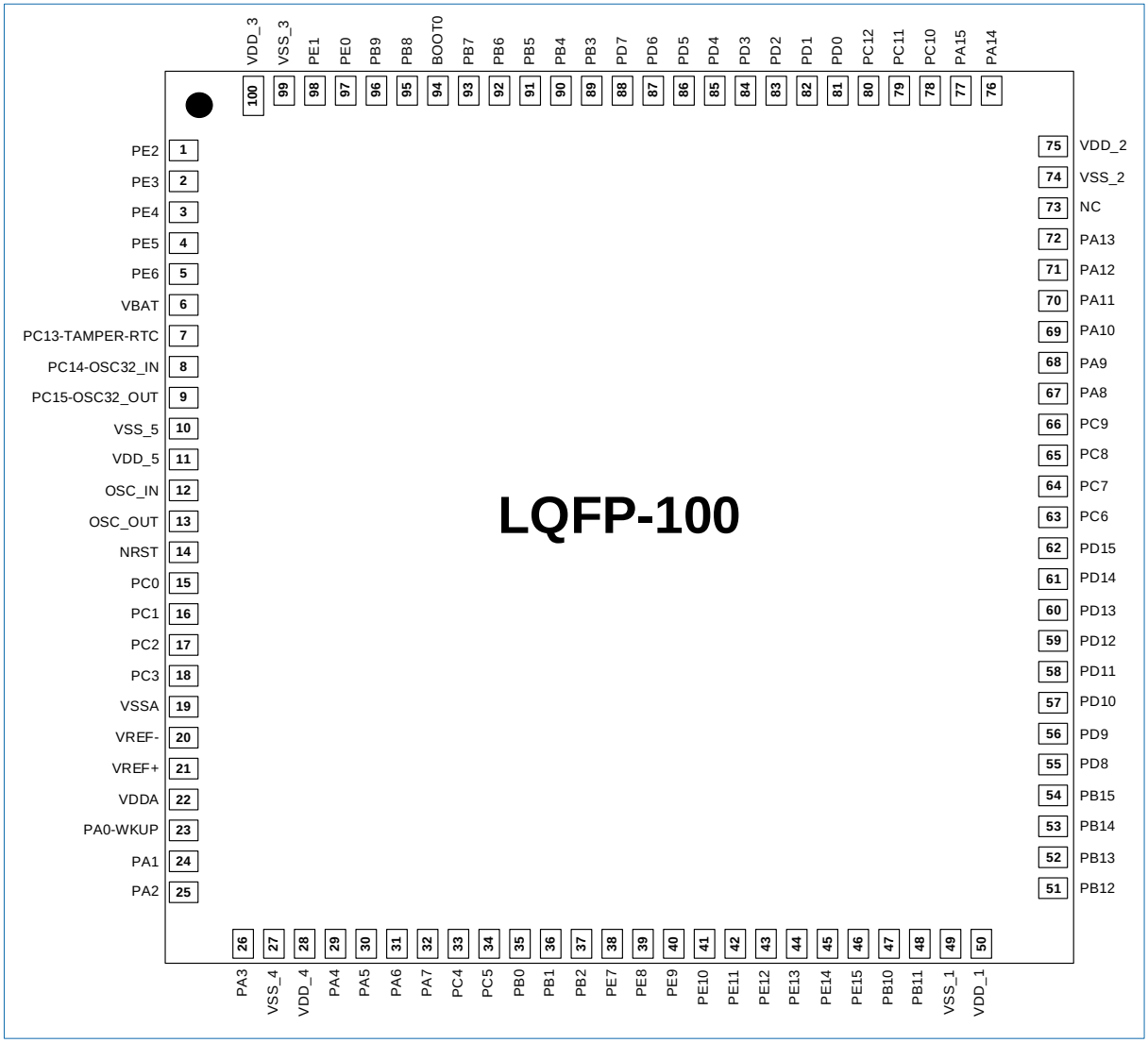

Figure 6-2 LQFP100 package pinout

6.3 Pin description

Table 6-1 shows pin description of LQFP64 and LQFP100 package.

Table 6-1 HK32F103xCxDxE LQFP64/LQFP100 pin descriptions

LQFP64	LQFP100	Pin Name	Type	Level	Main function	Alternate functions	
						Default	Remap
	1	PE2	I/O (1)	-	PE2	TRACECKO/FSMC_A23 ADC2_BGRBUF	TXEV/EXTIN2
	2	PE3	I/O	-	PE3	TRACED0/FSMC_A19 ADC2_AIN18	TXEV/EXTIN3
	3	PE4	I/O	-	PE4	TRACED1/FSMC_A20 ADC3_BGRBUF	TXEV/EXTIN4
	4	PE5	I/O	-	PE5	TRACED2/FSMC_A21 ADC3_AIN18	TXEV/EXTIN5
	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	TXEV/EXTIN6

LQFP64	LQFP100	Pin Name	Type	Level	Main function	Alternate functions	
						Default	Remap
1	6	VBAT	S	-	VBAT		
2	7	PC13-TAMPER-RTC	I/O (2)	-	PC13	TAMPER-RTC/WKUP1/RTCO	TXEV/EXTIN13
3	8	PC14-OSC32_IN	I/O (2)	-	PC14	OSC32_IN/LSE_CKI	TXEV/EXTIN14
4	9	PC15-OSC32_OUT	I/O (2)	-	PC15	OSC32_OUT	TXEV/EXTIN15
	10	VSS_5	S	-	VSS_5		
	11	VDD_5	S	-	VDD_5		
5	12	OSC_IN	I	-	OSC_IN	OSC_IN/HSE_CKI CAN1_RX2	TXEV/PD02 EXTIN02
6	13	OSC_OUT	O	-	OSC_OUT	OSC_OUT CAN1_TX2	TXEV/PD12 EXTIN12
7	14	NRST	I/O	-	NRST		
8	15	PC0	I/O	-	PC0	ADC123_IN10 FSMC_A13	TXEV/EXTIN0 FSMC_NIORD
9	16	PC1	I/O	-	PC1	ADC123_IN11	TXEV/EXTIN1
10	17	PC2	I/O	-	PC2	ADC123_IN12	TXEV/EXTIN2
11	18	PC3	I/O	-	PC3	ADC123_IN13	TXEV/EXTIN3
12	19	VSSA	S	-	VSSA		
	20	VREF-	S	-	VREF-		
	21	VREF+	S	-	VREF+		
13	22	VDDA	S	-	VDDA		
14	23	PA0-WKUP	I/O (2)	-	PA0	WKUP0/USART2_CTS/ADC123_IN0 TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR/EXTIN0	TXEV FSMC_NE4
15	24	PA1	I/O	-	PA1	USART2_RTS/ADC123_IN1 TIM5_CH2/TIM2_CH2/EXTIN1 RCC_CKI0	TXEV FSMC_A14
16	25	PA2	I/O	-	PA2	USART2_TX/TIM5_CH3 ADC123_IN2/TIM2_CH3/EXTIN2	TXEV
17	26	PA3	I/O	-	PA3	USART2_RX/TIM5_CH4 ADC123_IN3/TIM2_CH4/EXTIN3	TXEV FSMC_A15
18	27	VSS_4	S	-	VSS_4		
19	28	VDD_4	S	-	VDD		

LQFP64	LQFP100	Pin Name	Type	Level	Main function	Alternate functions	
						Default	Remap
					_4		
20	29	PA4	I/O	-	PA4	SPI1_NSS/USART2_CK DAC_OUT1/ADC12_IN4/EXTIN4 /I2S1_WS/TIM5_ETR	TXEV
21	30	PA5	I/O	-	PA5	SPI1_SCK/DAC_OUT2 ADC12_IN5/EXTIN5 /I2S1_CK	TXEV
22	31	PA6	I/O	-	PA6	SPI1_MISO/TIM8_BKIN ADC12_IN6/TIM3_CH1/EXTIN6	TXEV/TIM1_BKIN
23	32	PA7	I/O	-	PA7	SPI1_MOSI/TIM8_CH1N/ADC12_IN7/TIM3_CH2/EXTIN7 /I2S1_SD	TXEV/TIM1_CH1N FSMC_A0
24	33	PC4	I/O	-	PC4	ADC12_IN14 /I2S1_MCK	TXEV/EXTIN4 FSMC_A1
25	34	PC5	I/O	-	PC5	ADC12_IN15	TXEV/EXTIN5 FSMC_A2
26	35	PB0	I/O [2]	-	PB0	ADC12_IN8/TIM3_CH3/TIM8_CH2N WKUP2	TXEV/TIM1_CH2N/EXTIN0 FSMC_A3
27	36	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4/TIM8_CH3N RCC_CKI1	TXEV/TIM1_CH3N/EXTIN1 FSMC_A4
28	37	PB2	I/O	FT	PB2	BOOT1	TXEV/EXTIN2 FSMC_A5
	38	PE7	I/O	FT	PE7	FSMC_D4	TXEV/TIM1_ETR/EXTIN7
	39	PE8	I/O	FT	PE8	FSMC_D5	TXEV/TIM1_CH1N/EXTIN8
	40	PE9	I/O	FT	PE9	FSMC_D6	TXEV/TIM1_CH1/EXTIN9
	41	PE10	I/O	FT	PE10	FSMC_D7	TXEV/TIM1_CH2N/EXTIN10
	42	PE11	I/O	FT	PE11	FSMC_D8	TXEV/TIM1_CH2/EXTIN11
	43	PE12	I/O	FT	PE12	FSMC_D9	TXEV/TIM1_CH3N/EXTIN12
	44	PE13	I/O	FT	PE13	FSMC_D10	TXEV/TIM1_CH3/EXTIN13
	45	PE14	I/O	FT	PE14	FSMC_D11	TXEV/TIM1_CH4/EXTIN14
	46	PE15	I/O	FT	PE15	FSMC_D12	TXEV/TIM1_BKIN/EXTIN15
29	47	PB10	I/O		PB10	I2C2_SCL/USART3_TX	TXEV/TIM2_CH3/EXTIN10 FSMC_INT2/
30	48	PB11	I/O		PB11	I2C2_SDA/USART3_RX	TXEV/TIM2_CH4/EXTIN11 FSMC_INT3
31	49	VSS_1	S		VSS_1		
32	50	VDD_1	S		VDD_1		
33	51	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/I2C2_SMBA/USART3_CK/TIM1_BKIN /ADC3_VOLTDIV	TXEV/EXTIN12
34	52	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK/USART3_CTS/TIM1	TXEV/EXTIN13

LQFP64	LQFP100	Pin Name	Type	Level	Main function	Alternate functions	
						Default	Remap
						_CH1N	
35	53	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N/USART3_RTS	TXEV/EXTIN14
36	54	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD/TIM1_CH3N USART4_CK	TXEV/EXTIN15 FSMC_INTR
	55	PD8	I/O	FT	PD8	FSMC_D13	TXEV/USART3_TX/EXTIN8
	56	PD9	I/O	FT	PD9	FSMC_D14	TXEV/USART3_RX/EXTIN9
	57	PD10	I/O	FT	PD10	FSMC_D15	TXEV/USART3_CK/EXTIN10
	58	PD11	I/O	FT	PD11	FSMC_A16_CLE	TXEV/USART3_CTS/EXTIN11
	59	PD12	I/O	FT	PD12	FSMC_A17_ALE	TXEV/TIM4_CH1/USART3_RTS/EXTIN12
	60	PD13	I/O	FT	PD13	FSMC_A18	TXEV/TIM4_CH2/EXTIN13
	61	PD14	I/O	FT	PD14	FSMC_D0	TXEV/TIM4_CH3/EXTIN14
	62	PD15	I/O	FT	PD15	FSMC_D1	TXEV/TIM4_CH4/EXTIN15
37	63	PC6	I/O	FT	PC6	I2S2_MCK/TIM8_CH1/SDIO_D6 USART4_CTS	TXEV/TIM3_CH1/EXTIN6 FSMC_A6
38	64	PC7	I/O	FT	PC7	I2S3_MCK/TIM8_CH2/SDIO_D7 RCC_CKI2/USART4_RTS	TXEV/TIM3_CH2/EXTIN7 FSMC_A7
39	65	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TXEV/TIM3_CH3/EXTIN8 FSMC_A8/USART1_CTS/USART5_TX
40	66	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TXEV/TIM3_CH4/EXTIN9 FSMC_A9/USART1_RTS/USART5_RX
41	67	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/MCO/EXTIN8	TXEV FSMC_A10
42	68	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2/EXTIN9	TXEV FSMC_A11
43	69	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3/EXTIN10	TXEV FSMC_A12
44	70	PA11	I/O	FT	PA11	USART1_CTS/USBDM/CAN1_RX/TIM1_CH4/EXTIN11	TXEV
45	71	PA12	I/O	FT	PA12	USART1_RTS/USBDP/CAN1_TX/TIM1_ETR/EXTIN12	TXEV
46	72	PA13	I/O	FT	JTMS-SWDIO		PA13 TXEV/ FSMC_NIORD
	73	NC					

LQFP64	LQFP100	Pin Name	Type	Level	Main function	Alternate functions	
						Default	Remap
47	74	VSS_2	S		VSS_2		
48	75	VDD_2	S		VDD_2		
49	76	PA14	I/O	FT	JTCK-SWCLK	EXTIN14 /USART5_CK	TXEV/PA14 FSMC_NIOWR USART2_CTS/I2C1_SMBA
50	77	PA15	I/O	FT	JTDI	SPI3_NSS/I2S3_WS/EXTIN15 /I2S1_WS	TXEV/TIM2_CH1_ETR/PA15/SPI1_NSS FSMC_NREG /USART2_RTS
51	78	PC10	I/O		PC10	USART4_TX/SDIO_D2	TXEV/USART3_TX/EXTIN10 FSMC_A24/USART2_TX
52	79	PC11	I/O		PC11	USART4_RX/SDIO_D3	TXEV/USART3_RX/EXTIN11 FSMC_A25/USART2_RX
53	80	PC12	I/O		PC12	USART5_TX/SDIO_CK	TXEV/USART3_CK/EXTIN12 FSMC_NE2_NCE3/USART2_CK
	81	PD0	I/O	FT	PD0	FSMC_D2	TXEV/CAN1_RX/EXTIN0
	82	PD1	I/O	FT	PD1	FSMC_D3	TXEV/CAN1_TX/EXTIN1
54	83	PD2	I/O		PD2	TIM3_ETR/USART5_RX/SDIO_CMD	TXEV/EXTIN2 FSMC_NE3_NCE4_1
	84	PD3	I/O	FT	PD3	FSMC_CLK USART5_CTS	TXEV/USART2_CTS/EXTIN3 SPI3_NSS/I2S3_WS
	85	PD4	I/O	FT	PD4	FSMC_NOE USART5_RTS	TXEV/USART2_RTS/EXTIN4 SPI3_SCK/I2S3_CK
	86	PD5	I/O	FT	PD5	FSMC_NWE	TXEV/USART2_TX/EXTIN5 SPI3_MISO
	87	PD6	I/O	FT	PD6	FSMC_NWAIT	TXEV/USART2_RX/EXTIN6 SPI3_MOSI/I2S3_SD
	88	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	TXEV/USART2_CK/EXTIN7
55	89	PB3	I/O		JTDO	SPI3_SCK/I2S3_CK ADC3_IN5	TXEV/PB3/TRACESWO/TIM2_CH2/SPI1_SCK/EXTIN3 I2S1_CK
56	90	PB4	I/O		NJTRST	SPI3_MISO ADC3_IN6	TXEV/PB4/TIM3_CH1/SPI1_MISO/EXTIN4
57	91	PB5	I/O		PB5	I2C1_SMBA/SPI3_MOSI/I2S3_SD /ADC3_IN7	TXEV/TIM3_CH2/SPI1_MOSI/EXTIN5 I2S1_SD
58	92	PB6	I/O		PB6	I2C1_SCL/TIM4_CH1 ADC3_IN8	TXEV/USART1_TX/EXTIN6 FSMC_NCE4_2/I2S1_MCK
59	93	PB7	I/O	FT	PB7	I2C1_SDA/FSMC_NADV/TIM4_CH2 RCC_CKI3	TXEV/USART1_RX/EXTIN7
60	94	BOOT0	I		BOOT0		
61	95	PB8	I/O		PB8	TIM4_CH3/SDIO_D4	TXEV/I2C1_SCL/CAN1_RX/EXTIN8 FSMC_CD/USART4_TX

LQFP64	LQFP100	Pin Name	Type	Level	Main function	Alternate functions	
						Default	Remap
62	96	PB9	I/O		PB9	TIM4_CH4/SDIO_D5	TXEV/I2C1_SDA/CAN1_TX/EXTIN9 USART4_RX
	97	PE0	I/O	FT	PE0	TIM4_ETR/FSMC_NBL0	TXEV/EXTIN0
	98	PE1	I/O	FT	PE1	FSMC_NBL1	TXEV/EXTIN1
63	99	VSS_3	S		VSS_3		
64	100	VDD_3	S	-	VDD_3		

(1). I= input, O=output, I/O= input/output, S=supply.

(2). Except for these pins, the other I/Os have the Schmitt function and can be configured via register.

7 Package characteristics

7.1 LQFP64

LQFP64 is a 10 x 10 mm and 0.5 mm pitch package.

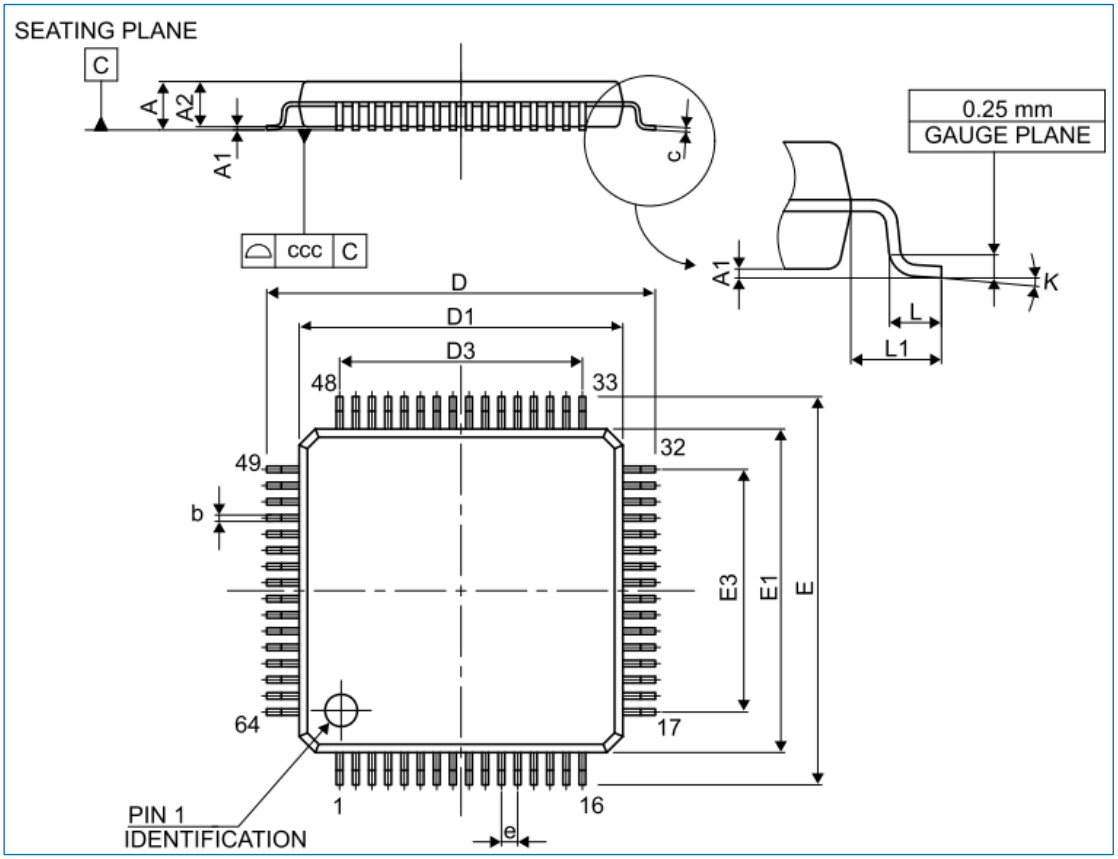

Figure 7-1 LQFP64 package outline

Table 7-1 LQFP64 package parameters

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

7.1.1 Recommended footprint

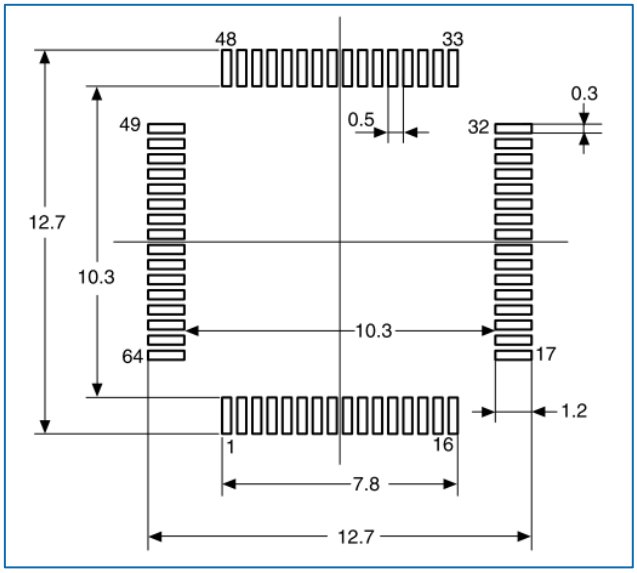

Figure 7-2 LQFP64 recommended footprint

7.2 LQFP100

LQFP100 is a 14 mm x 14 mm and 0.5 mm pitch package.

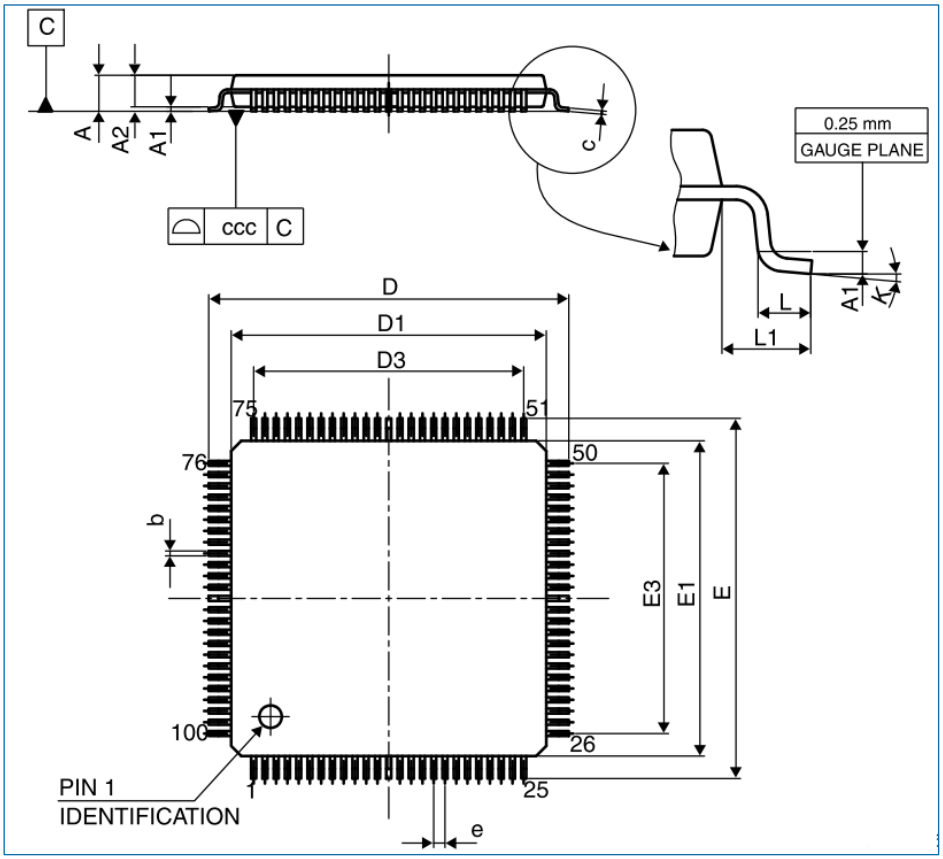

Figure 7-3 LQFP100 package outline

Table 7-2 LQFP100 package parameters

Symbol	millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

7.2.1 Recommended footprint

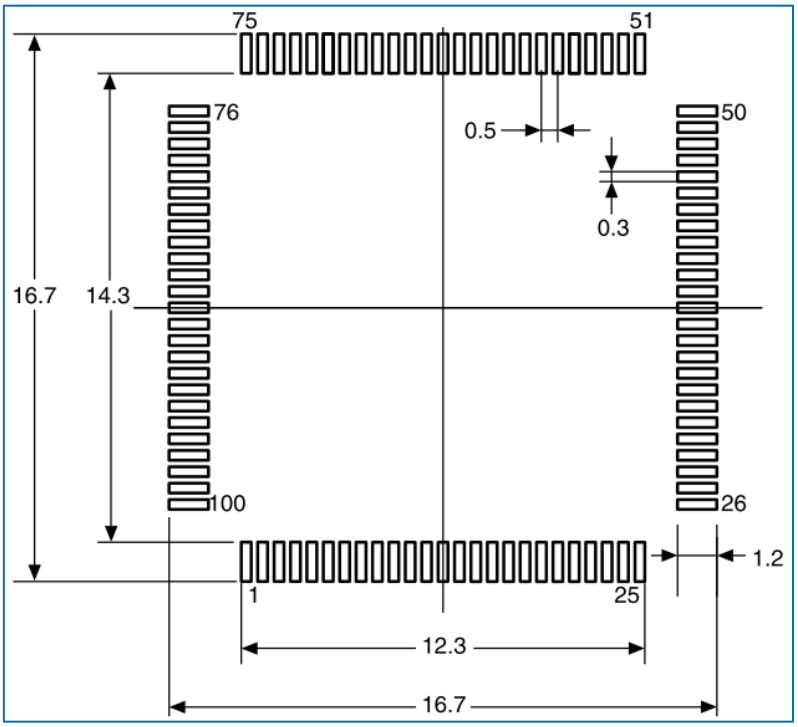

Figure 7-4 LQFP100 recommended footprint

8 Ordering information

Table 8-1 HK32F103xCxDxE ordering information

HK32F103xCxDxE series	Packaging	Comments
HK32F103RCT6	Tape and reel /Tray	-
HK32F103RDT6	Tape and reel/Tray	-
HK32F103RET6	Tape and reel/Tray	-
HK32F103VCT6	Tape and reel/Tray	-
HK32F103VDT6	Tape and reel/Tray	-
HK32F103VET6	Tape and reel/Tray	-

9 Glossary and Abbreviations

Name	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-Wakeup
CRC	Cyclic Redundancy Check
CSS	Clock Security System
DMA	Direct Memory Access
EXTI	External Interrupts and Events Controller
FSMC	Flexible Static Memory Controller
GPIO	General Purpose Input Output
HSE	High Speed External (Clock Signal)
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-Speed Internal (Clock Signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-Down Reset
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous Asynchronous Receiver Transmitter
WWDG	Window Watchdog

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