DIO74546

Low Voltage 4-Channel I²C and SMBus Switch with Reset Function

Description

The DIO74546 is a four-channel bidirectional translating switch controlled via the I²C bus. The upstream pair, SCL/SDA, can be connected to four downstream pairs or channels. Users can select any individual SCn/SDn channel or a combination of channels by programming the control register.

The switch has an active-low reset input that allows it to recover if one of the downstream I²C buses is stuck in a low state. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and deselects all the channels, as does the internal power-on reset function.

The pass gates of the switches are designed to limit the maximum high voltage that passes through the VCC pin. This feature allows the use of different bus voltages on each pair, so that 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5 V tolerant.

Features

- 1-of-4 bidirectional translating switches
- I²C bus and SMBus compatible
- Active-low reset input
- Three address pins, allowing up to four DIO74546 devices on the I²C bus
- Channel selection via I²C bus, in any combination
- Power-up with all switch channels deselected
- Low R_{ON} switches
- Allows voltage-level translation between 1.8 V, 2.5 V, 3.3 V, and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Power-supply voltage range: 1.65 V to 5.5 V
- 5.5 V tolerant inputs
- 0 to 400 kHz clock frequency

Applications

- Servers
- Routers (telecom switching equipment)
- Factory automation
- Products with I²C slave address conflicts (multiple, identical temp sensors)

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Ordering Information

Part Number	Top Marking	RoHS	T_A	Package	
DIO74546CT16	DGDE4F	Green	-40 to +125°C	TSSOP16	Tape & Reel, 2500
DIO74546CS16	DGDE4F	Green	-40 to +125°C	SOP16	Tape & Reel, 2500

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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Table of Contents

1. Pin Assignment and Functions 1
2. Absolute Maximum Ratings 2
3. Recommended Operating Condition 2
4. ESD Ratings 3
5. Thermal Considerations 3
6. Electrical Characteristics 3
7. Reset Timing Requirements 5
8. Switching Characteristics 5
9. Typical Characteristics 6
10. Parameter Measurement Information 7
11. Block Diagram 8
12. Function Description 8
12.1. $\overline{\text{RESET}}$ input 9
12.2. Power-on reset 9
12.3. I^2C interface 9
12.4. Control register 12
13. Application Information 14
13.1. Typical application 14
13.2. Design requirements 14
13.3. Detailed design procedure 15
13.4. Application curves 15
13.5. Power-on reset requirements 16
14. Layout Guidelines 18
15. Physical Dimensions 19
15.1. TSSOP16 19
15.2. SOP16 20

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List of Figures

Figure 1. V_{OL} vs. I_{OL} at three V_{CC} levels 6
Figure 2. I_{CC} vs. V_{CC} at three temperature points 6
Figure 3. R_{ON} vs. V_{CC} at three temperature 6
Figure 4. V_{PASS} vs. V_{CC} at three temperature points 6
Figure 5. I^2C load circuit, byte descriptions, and voltage waveforms 7
Figure 6. Reset timing 7
Figure 7. Bit transfer 9
Figure 8. Definition of start and stop conditions 10
Figure 9. System configuration 10
Figure 10. Acknowledgment on the I^2C Bus 11
Figure 11. Write control register 11
Figure 12. Read control register 11
Figure 13. Address 12
Figure 14. Control register 13
Figure 15. Typical application schematic 14
Figure 16. Standard mode vs. Fast mode 15
Figure 17. Minimum pull-up resistance vs Pull-up reference voltage 15
Figure 18. V_{CC} is lowered below the POR threshold, then ramped back up to V_{CC} 16
Figure 19. Glitch width and glitch height 17
Figure 20. V_{POR} 17

List of Table

Table 1. Address reference 12
Table 2. Control register write (channel selection), control register read (channel status) 13
Table 3. Recommended supply sequencing and ramp rates(1) 16

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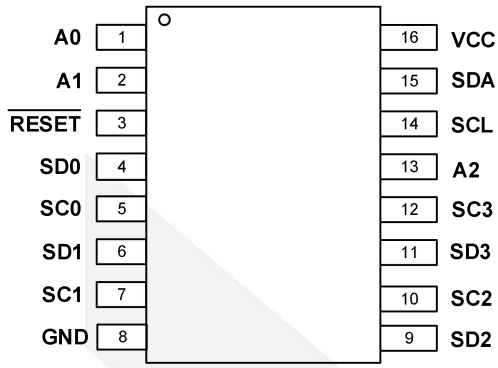
1. Pin Assignment and Functions



TSSOP16 / SOP16 (Top view)

Name	I/O	Description
A0	I	Address input 0. Connect directly to V_{CC} or ground
A1	I	Address input 1. Connect directly to V_{CC} or ground
A2	I	Address input 2. Connect directly to V_{CC} or ground
GND	-	Ground
$\overline{RESET}$	I	Active-low reset input. Connect to V_{CC} or V_{DPUM}(1) through a pull-up resistor, if not used.
SD0	I/O	Serial data 0. Connect to V_{DPU0}(1) through a pull-up resistor
SC0	I/O	Serial clock 0. Connect to V_{DPU0}(1) through a pull-up resistor
SD1	I/O	Serial data 1. Connect to V_{DPU1}(1) through a pull-up resistor
SC1	I/O	Serial clock 1. Connect to V_{DPU1}(1) through a pull-up resistor
SD2	I/O	Serial data 2. Connect to V_{DPU2}(1) through a pull-up resistor
SC2	I/O	Serial clock 2. Connect to V_{DPU2}(1) through a pull-up resistor
SD3	I/O	Serial data 3. Connect to V_{DPU3}(1) through a pull-up resistor
SC3	I/O	Serial clock 3. Connect to V_{DPU3}(1) through a pull-up resistor
SCL	I/O	Serial clock bus. Connect to V_{DPUM}(1) through a pull-up resistor
SDA	I/O	Serial data bus. Connect to V_{DPUM}(1) through a pull-up resistor
VCC	Power	Supply voltage

Note:
(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C master reference voltage and V_{DPU0}-V_{DPU3} are the slave channel reference voltages.

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2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		-0.5	7	V
V_{IN}	Input voltage(1)		-0.5	7	V
I_{IN}	Input current		-20	20	mA
I_{OUT}	Output current		-25		mA
I_{CC}	Supply current		-100	100	mA
T_{STG}	Storage temperature		-65	150	°C
T_J	Max junction temperature	V_{CC} ≤ 3.6 V		130	°C
		V_{CC} ≤ 5.5 V		90	

Note:
(1) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.

3. Recommended Operating Condition

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage	-40°C ≤ T_A ≤ 85°C	1.65	5.5	V
		85°C < T_A ≤ 125°C	1.65	3.6	
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	6	V
		A2-A0, $\overline{\text{RESET}}$	0.7 × V_{CC}	V_{CC} + 0.5	
V_{IL}	Low-level input voltage	SCL, SDA	-0.5	0.3 × V_{CC}	V
		A2-A0, $\overline{\text{RESET}}$	-0.5	0.3 × V_{CC}	
T_A	Operating free-air temperature	3.6 V < V_{CC} ≤ 5.5 V	-40	85	°C
		1.65 V ≤ V_{CC} ≤ 3.6 V	-40	125	

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4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
ESD	Human body model	±8000	V
	Charged-device model	±2000	V

5. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Metric	Value		Unit
		TSSOP16	SOP16	
$R_{\theta JA}$	Junction-to-air thermal resistance	95	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	55	60	

6. Electrical Characteristics

The values are obtained under these conditions unless otherwise specified: V_{CC} = 1.65 V to 5.5 V. Typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, or 5 V), T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC}	Min	Typ	Max	Unit
V_{PORR}	Power-on reset voltage, V_{CC} rising	No load, V_{IN} = V_{CC} or GND(1)			1.3	1.55	V
V_{PORF}	Power-on reset voltage, V_{CC} falling(2)	No load, V_{IN} = V_{CC} or GND(1)		0.85	1.1		V
V_{pass}	Switch output voltage	$V_{IN(sw)}$ = V_{CC}, I_{SWout} = -100 μA	5 V		3.5		V
			4.5 V to 5.5 V	2.9		4	
			3.3 V		2		
			3 V to 3.6 V	1.6		2.5	
			2.5 V		1.4		
			2.3 V to 2.7 V	1.1		2	
			1.8 V		0.8		
			1.65 V to 1.95 V	0.5		1.2	
I_{OL}	SDA	V_{OL} = 0.4 V	1.65 V to 5.5 V	3	15		mA
		V_{OL} = 0.6 V		6	20		
I_{IN}	SCL, SDA	V_{IN} = V_{CC} or GND(1)	1.65 V to 5.5 V	-1		1	μA
	SC3-SC0, SD3-SD0			-1		1	
	A2-A0			-1		1	
	$\overline{\text{RESET}}$			-1		1	

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Symbol	Parameter	Test Conditions	V_{CC}	Min	Typ	Max	Unit
I_{CC}	Operating mode	V_{IN} = V_{CC} or GND(1), I_{OUT} = 0 $t_{r,max}$ = 300 ns, f_{SCL} = 400 kHz	5.5 V		50		μA
			3.6 V		21		
			2.7 V		19		
			1.65 V		10		
		V_I = V_{CC} or GND(1), I_{OUT} = 0 $t_{r,max}$ = 1 μs, f_{SCL} = 100 kHz	5.5 V		4		
			3.6 V		2		
			2.7 V		1.5		
			1.65 V		1		
	Standby mode	V_{IN} = GND(3), I_{OUT} = 0, -40°C ≤ T_A ≤ 85°C, Low inputs	5.5 V		0.45	2	
			3.6 V		0.3	2	
			2.7 V		0.22	1	
			1.65 V		0.13	1	
		V_{IN} = V_{CC}, I_{OUT} = 0, -40°C ≤ T_A ≤ 85°C, High inputs	5.5 V		0.45	2	
			3.6 V		0.3	2	
			2.7 V		0.22	1	
			1.65 V		0.13	1	
		V_{IN} = V_{CC} or GND, I_{OUT} = 0, 85°C <T_A ≤ 125°C, Low and high inputs	3.6 V		0.54	2	
			2.7 V		0.45	1.5	
			1.65 V		0.31	1	
ΔI_{CC}	Supply-currentchange, SCL, SDA	SCL or SDA input at 0.6 V, other inputs at V_{CC} or GND(1)	1.65 V to 5.5 V		3		μA
		SCL or SDA input at V_{CC} - 0.6 V,other inputs at V_{CC} or GND(1)			3		
C_{IN}	A2-A0	V_{IN} = V_{CC} or GND(1)	1.65 V to 5.5 V		4		pF
	$\overline{RESET}$				4		
$C_{IO(OFF)}$ (3)	SCL, SDA	V_{IN} = V_{CC} or GND(1), switch off	1.65 V to 5.5 V		20		pF
	SC3-SC0, SD3-SD0				5.5		pF
R_{ON}	Switch-on resistance	V_{OUT} = 0.4 V, I_{OUT} = 15 mA	4.5 V to 5.5 V	2.5	4.5	7	Ω
			3 V to 3.6 V	3	6	10	Ω
		V_{OUT} = 0.4 V, I_{OUT} = 10 mA	2.3 V to 2.7 V	4	8	12	Ω
			1.65 V to 1.95 V	6.5	16	25	Ω

Note:

(1) $\overline{RESET}$ = V_{CC} (held high) when all other input voltages, V_{IN} = GND.

(2) The power-on reset circuit resets the I^2C bus logic with V_{CC} < V_{PORF}.

(3) $C_{IO(ON)}$ depends on internal capacitance and external capacitance added to the SCn lines when channels(s) are ON.

(4) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(5) Specifications subject to change without notice.

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7. Reset Timing Requirements

Over recommended operating free-air temperature range (unless otherwise noted).

Symbol	Parameter		Min	Max	Unit
$t_{W(L)}$(1)	Pulse duration, $\overline{\text{RESET}}$ low	V_{CC} ≥ 2.5 V	18		ns
		1.65 V ≤ V_{CC} < 2.5 V	28		
$t_{REC(STA)}$(1)	Recovery time from $\overline{\text{RESET}}$ to start		0		

Note:

(1) Guaranteed by design.

8. Switching Characteristics

Over recommended operating free-air temperature range, C_L ≤ 100 pF unless otherwise noted .

Symbol	Parameter		From (input)	To (output)	Min	Typ	Max	Unit
t_{pd} (1)	Propagation delay time	R_{ON} = 16 Ω, C_L = 15 pF	SDA or SCL	SDn or SCn		0.24		ns
		R_{ON} = 16 Ω, C_L = 50 pF				0.8		
t_{rst}(2)(3)	$\overline{\text{RESET}}$ time (SDA clear)		$\overline{\text{RESET}}$	SDA			500	ns

Note:

(1) The propagation delay is the calculated RC time constant of the typical switch on-state resistance and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(2) t_{rst} is the propagation delay measured from the time the $\overline{\text{RESET}}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of $t_{W(L)}$.

(3) Guaranteed by design.

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9. Typical Characteristics

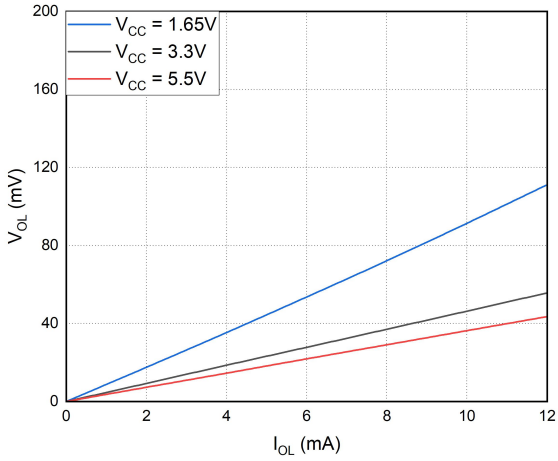

Figure 1. V_{OL} vs. I_{OL} at three V_{CC} levels

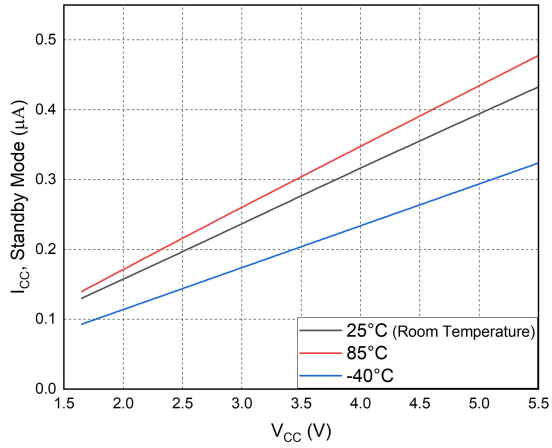

Figure 2. I_{CC} vs. V_{CC} at three temperature points

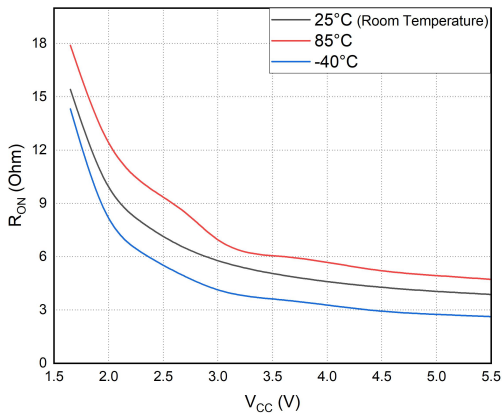

Figure 3. R_{ON} vs. V_{CC} at three temperature

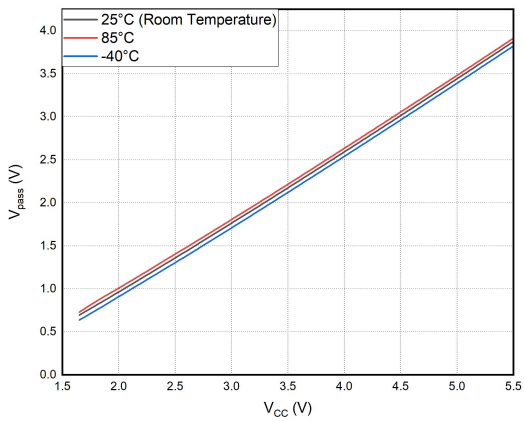

Figure 4. V_{PASS} vs. V_{CC} at three temperature points

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10. Parameter Measurement Information

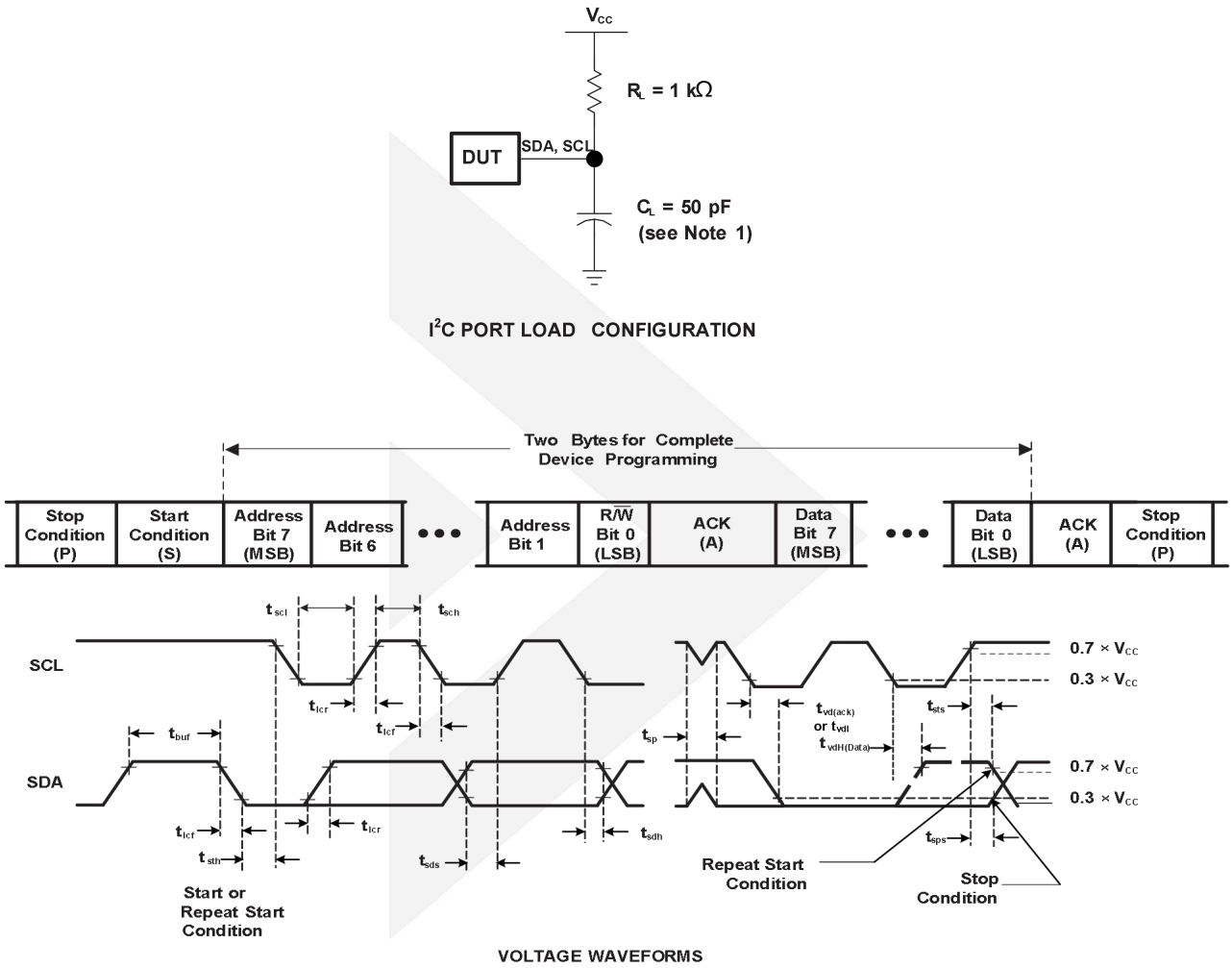

Figure 5. I²C load circuit, byte descriptions, and voltage waveforms

Note:

(1) C_L includes probe and jig capacitance.

(2) All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

(3) The outputs are measured one at a time, with one transition per measurement.

(4) Not all parameters and waveforms are applicable to all devices.

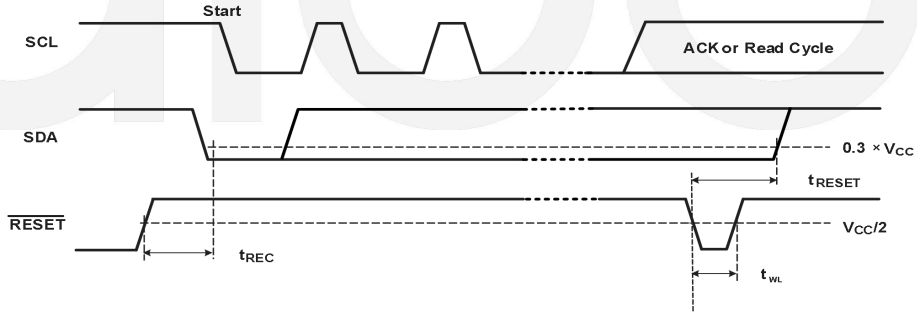

Figure 6. Reset timing

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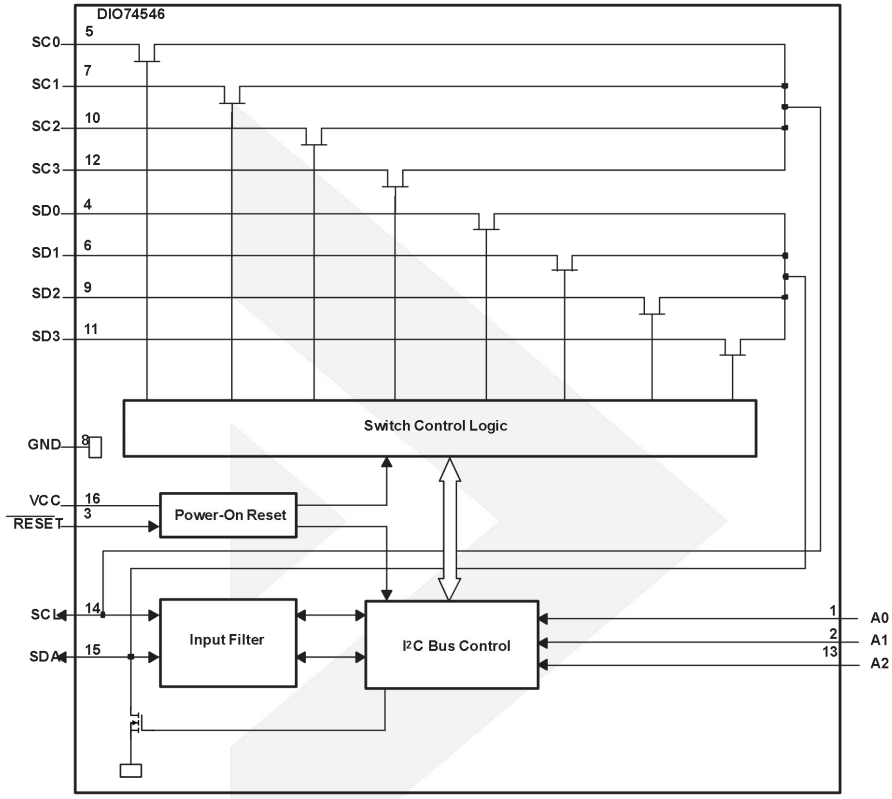
11. Block Diagram



12. Function Description

The DIO74546 is a device that helps to connect multiple devices by using a communication protocol called I^2C. It has four channels that can connect to four different devices. The user can choose to connect to any one of the four channels or a combination of them.

The device also has a feature that allows it to recover from errors. This feature resets the device and allows it to function properly if one of the channels stuck in a low state. The device can also be reset by turning off and on the power supply, known as a power-on reset (POR). Both the $\overline{\text{RESET}}$ function and a POR will cause all channels to be deselected.

The device is controlled by a master device that communicates with multiple slave devices. The user can select which channels to use by writing or reading a control register.

The same I^2C master device that communicates with multiple I^2C slaves also controls the connections of the I^2C data path. With the acknowledgement of the slave address (which can be selected through the A0 and A1 pins), users can write to or read from a single 8-bit control register to choose the desired channels.

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The DIO74546 can be used to connect devices that have different voltage levels. This is done by adjusting the voltage level on each channel using external pull-up resistors. It allows devices with 1.8 V, 2.5 V, or 3.3 V to communicate with devices that have a voltage of 5 V.

12.1. $\overline{\text{RESET}}$ input

To recover the device from a bus-fault condition, pull the $\overline{\text{RESET}}$ low. When this signal is asserted low for a minimum of t_{WL}, the DIO74546 resets its registers and I^2C state machine and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to VCC through a pull-up resistor.

12.2. Power-on reset

POR is a function that resets a state machine and all internal registers of the device to a default state when power is first applied. This ensures that the device starts with a known and reliable state, which can help prevent errors and malfunctions. When power is applied to VCC, an internal power-on reset holds the DIO74546 in a reset condition until V_{CC} has reached V_{POR}. At this point, the reset condition is ended, and the DIO74546 registers and I^2C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below V_{POR} to reset the device again.

12.3. I^2C interface

The I^2C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). The SDA line carries data between the devices, while the SCL line synchronizes the data transfer between the devices. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device.

In I^2C bus, "busy" refers to the state of the bus when it is currently being used by one or more devices to transmit data. When the bus is busy, other devices that want to initiate a data transfer must wait until the bus becomes free before they can start their transfer. The bus can become busy in several ways, such as when a device is currently transmitting data, receiving data, or holding the bus to perform a specific operation. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse because changes in the data line at this time are interpreted as control signals (see Figure 7).

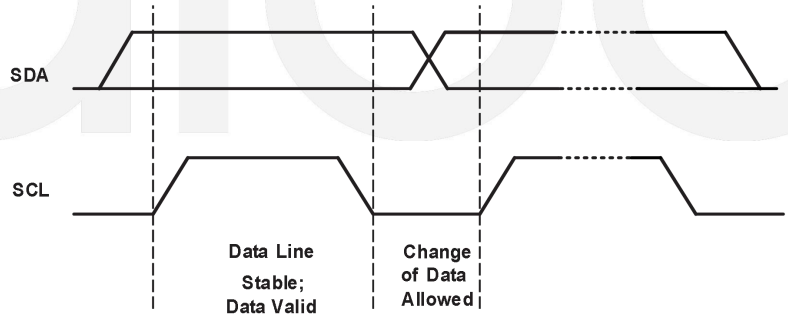

Figure 7. Bit transfer

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Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 8).

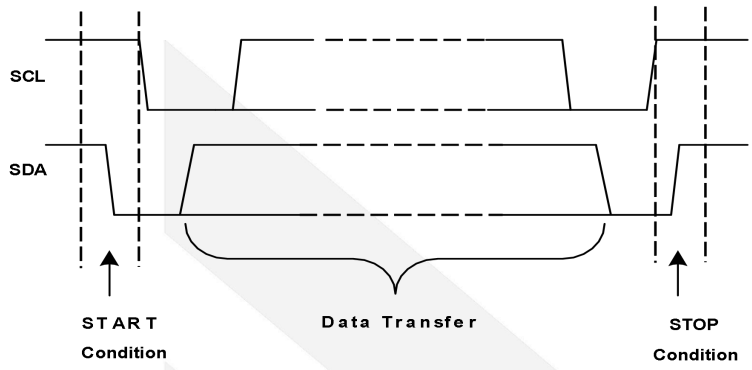

Figure 8. Definition of start and stop conditions

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 9).

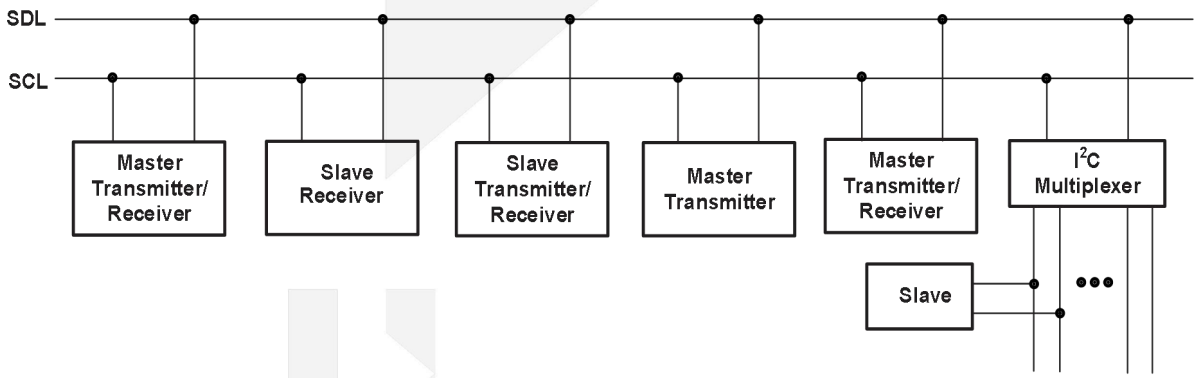

Figure 9. System configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

If a slave receiver is addressed, it must generate an ACK after receiving each byte, while a master must generate an ACK after receiving each byte clocked out of the slave transmitter. During the ACK clock pulse, the device acknowledging must pull down the SDA line so that it remains stable low during the high pulse of the ACK-related clock period. The setup and hold times must be taken into account. See Figure 10 for more information.

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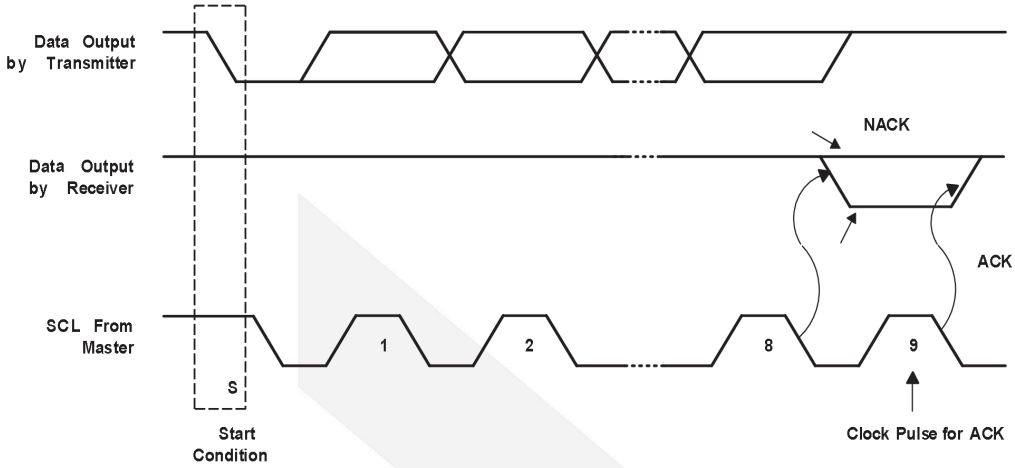

Figure 10. Acknowledgment on the I²C Bus

Data is transmitted to the DIO74546 control register by using the write mode shown in Figure 11.

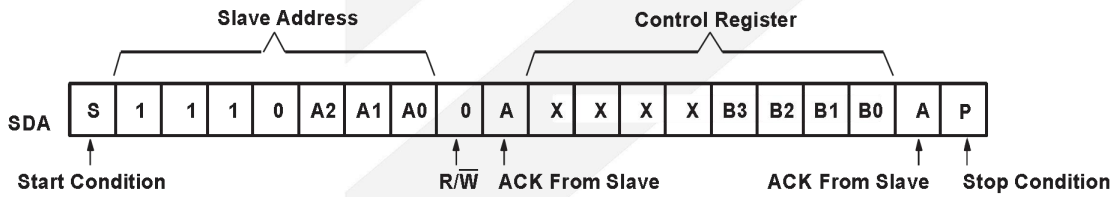

Figure 11. Write control register

Data is read from the DIO74546 control register by using the read mode shown in Figure 12.

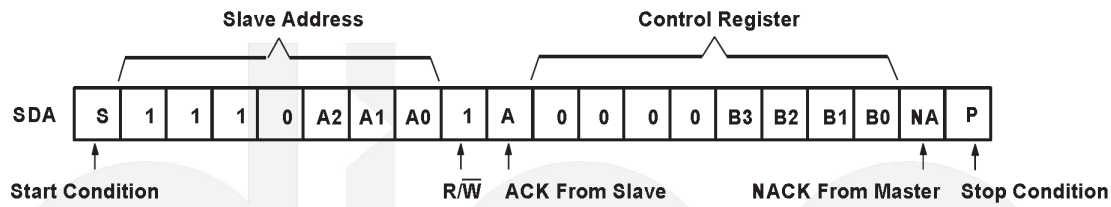

Figure 12. Read control register

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12.4. Control register

12.4.1. Device address

After initiating communication, the master device on the I²C bus needs to specify which slave device it wants to communicate by sending its address. The specific address for the DIO74546 is provided in Figure 13. The device doesn't have any internal pull-up resistors for its address pins (A0 and A1) to save power, so external pull-up resistors need to be used to set them to high or low.

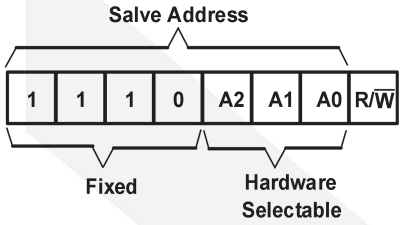

Figure 13. Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

Table 1. Address reference

Inputs			I²C Bus Slave Address
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

12.4.2. Control register description

When the salve address is acknowledged by the slave register, the bus master sends a byte to the DIO74546. The byte is stored in the control register (see Figure 14). If the DIO74546 receives multiple bytes, the register will save the last byte received. This register can be written and read through the I²C bus.

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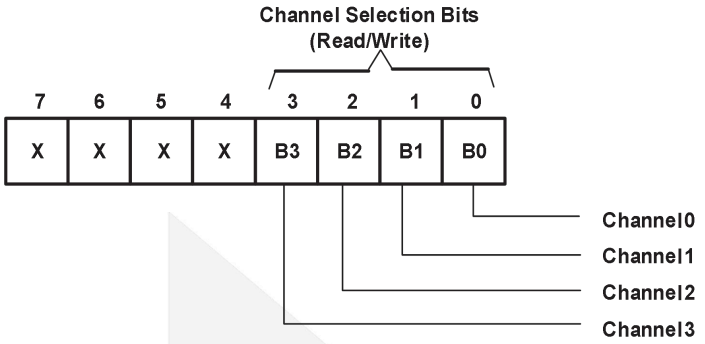

Figure 14. Control register

12.4.3. Control register definition

The control register selects one or more SCn/SDn downstream pairs, or channels (see Table 2). This register is written after the DIO74546 is addressed. The four LSBs of the control byte are used to determine the selection of channel or channels. Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 and 2 are enabled. Do not exceed the maximum bus capacity. The selected channel is active after a stop condition has been placed on the I^2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is active to avoid false conditions at the time of connection. A stop condition always must occur right after the acknowledge cycle.

Table 2. Control register write (channel selection), control register read (channel status)

B7	B6	B5	B4	B3	B2	B1	B0	Command
x	x	x	x	x	x	x	0	Channel 0 disable
							1	Channel 0 enable
x	x	x	x	x	x	0	x	Channel 1 disable
						1		Channel 1 enable
x	x	x	x	x	0	x	x	Channel 2 disable
					1			Channel 2 enable
x	x	x	x	0	x	x	x	Channel 3 disable
				1				Channel 3 enable
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

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13. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

Applications of the DIO74546 contains an I²C (or SMBus) master device and four I²C slave devices. The downstream channels can resolve I²C slave address conflicts. In an application where the I²C bus contain many additional slave devices that do not result in I²C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See Design Requirements and Detailed Design Procedure).

13.1. Typical application

A typical application of the DIO74546 contains anywhere from one to five separate data pull-up voltages, V_{DPUX}. V_{DPUM} is for the master device and V_{DPU0} to V_{DPU3} are for each of the selectable slave channels. V_{pass} is equal to V_{DPUX} when the master device and all slave devices operate at the same voltage. If the voltage translation is necessary, additional design requirements must be considered (See Design Requirements).

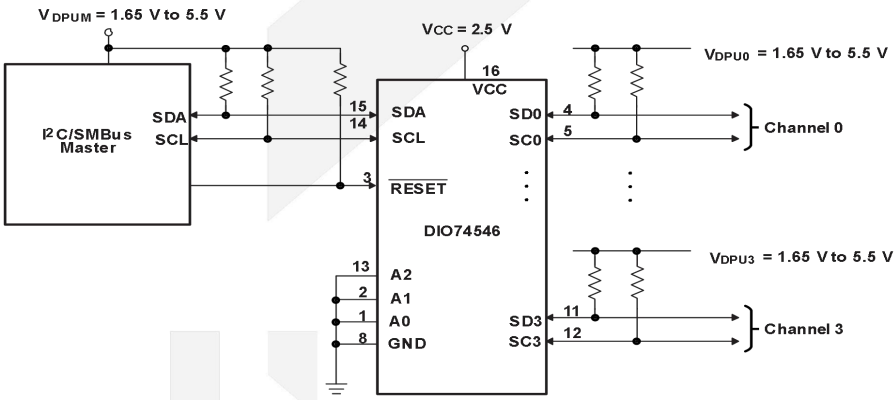

Figure 15. Typical application schematic

13.2. Design requirements

To control the slave address of the DIO74546, use the hardware selectable pins A0, A1, and A2. These pins may be tied directly to GND or VCC in the application.

If multiple slave channels is activated simultaneously, then the total I_{OL} from SCL/SDA to GND on the master side is the sum of the currents through all pull-up resistors, R_p.

The construction of pass-gate transistors of the DIO74546 can make the VCC voltage be used to limit the maximum voltage that is passed from one I²C bus to another.

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13.3. Detailed design procedure

As soon as all the slaves are assigned to the appropriate slave channels and bus voltages are identified, select the pull-up resistors, R_p, for each of the buses appropriately. The minimum pull-up resistance can be calculated from the following equation.

$$R_{P(\min)} = \frac{V_{DPUX} - V_{OL(\max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance can be calculated from the following equation.

$$R_{P(\max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

Where

t_r is the maximum rise time, 300 ns for fast-mode operation, f_{SCL} = 400 kHz
C_b is the bus capacitance

In fast-mode operation, the maximum bus capacitance for an I^2C bus must not exceed 400 pF. The bus capacitance can be approximated by adding the capacitance of the DIO74546, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

13.4. Application curves

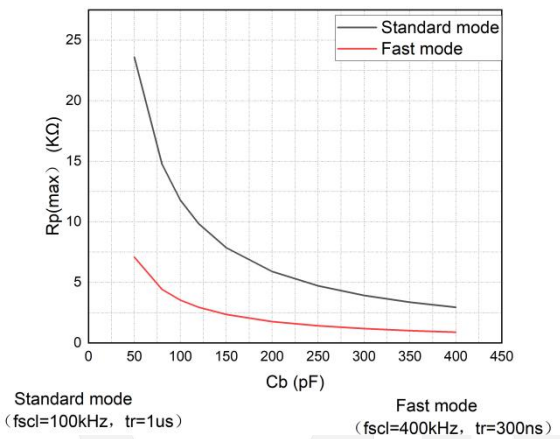
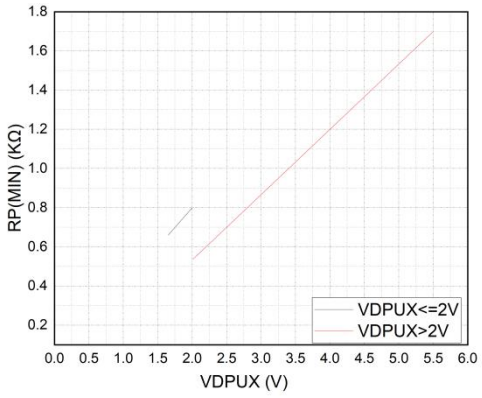


Figure 16. Standard mode vs. Fast mode



V_{OL} = 0.2×V_{DPUX}, I_{OL} = 2 mA when V_{DPUX} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

Figure 17. Minimum pull-up resistance vs Pull-up reference voltage

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13.5. Power-on reset requirements

When the DIO74546 is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I^2C bus logic is initialized properly.

In the event of a glitch or data corruption, the DIO74546 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application. A power-on reset is shown in Figure 18.

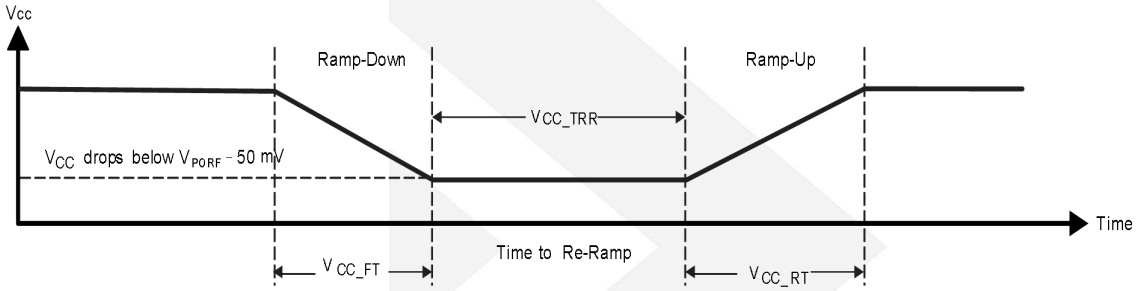

Figure 18. V_{CC} is lowered below the POR threshold, then ramped back up to V_{CC}

Table 3 specifies the performance of the power-on reset feature for the DIO74546 for both types of power-on reset.

Table 3. Recommended supply sequencing and ramp rates(1)

Symbol	Parameter	Min	Typ	Max	Unit
VCC_FT(2)	Fall time	1		100	ms
VCC_RT(2)	Rise time	0.1		100	ms
VCC_TRR(2)	Time to re-ramp (when VCC drops below VPORF(min) – 50 mV or when VCC drops to GND)	40			µs
VCC_GH(3)	Level that VCC can glitch down to, but not cause a functional disruption when VCC_GW = 1 µs			1.2	V
VCC_GW(3)	Glitch width that will not cause a functional disruption when VCC_GH = 0.5 × VCC			10	µs
VPORF(4)	Voltage trip point of POR on falling VCC	0.8		1.25	V
VPORR(4)	Voltage trip point of POR on rising VCC	1.05		1.5	V

Note:

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C.

(2) See Figure 18

(3) See Figure 19

(4) See Figure 20

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Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 19 and Table 3 provide more information on how to measure these specifications.

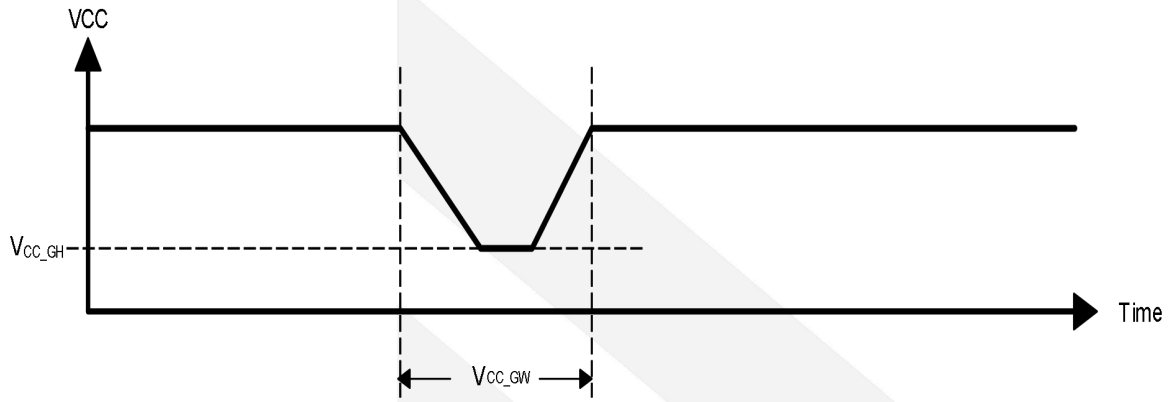

Figure 19. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the VCC being lowered to or from 0. Figure 20 and Table 3 provide more details on this specification.

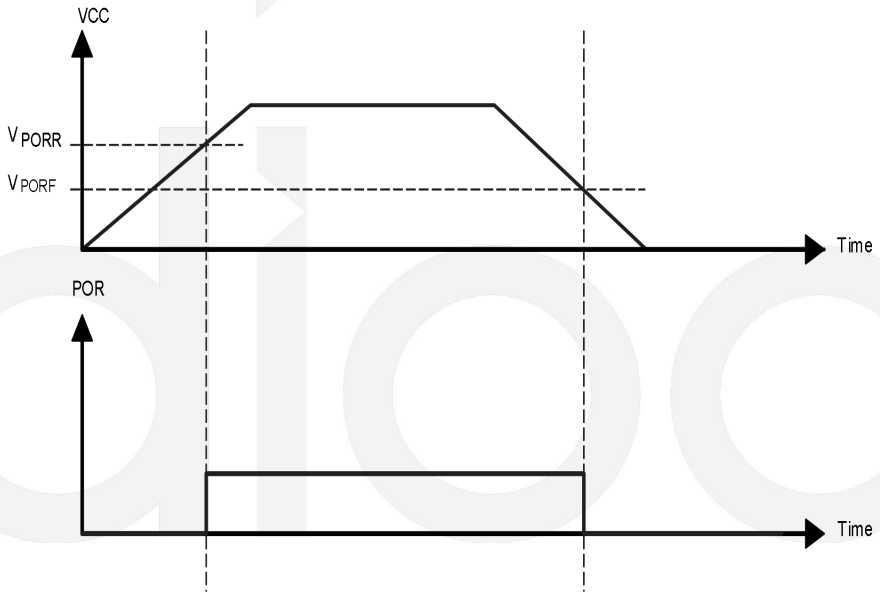

Figure 20. V_{POR}

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14. Layout Guidelines

For PCB layout of the DIO74546, follow the common PCB layout practices. However, additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds. Use a dedicated ground plane on an inner layer of the board. Pins that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. To control the voltage on the VCC pin, use by-pass and de-coupling capacitors. Use a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

If voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. If voltage translation is required, V_{DPUM}, V_{DPU0}, V_{DPU1}, V_{DPU2}, and V_{DPU3} can all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I^2C bus capacitance added by PCB parasitics, minimize the length of data lines (SCn and SDn) and the widths of the trace (for example, 5-10 mils depending on copper weight).

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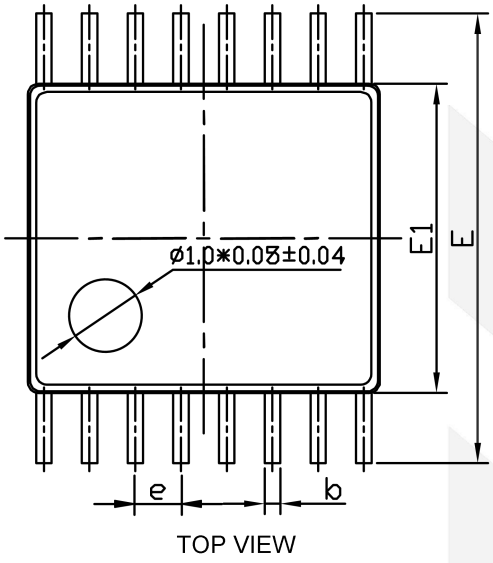
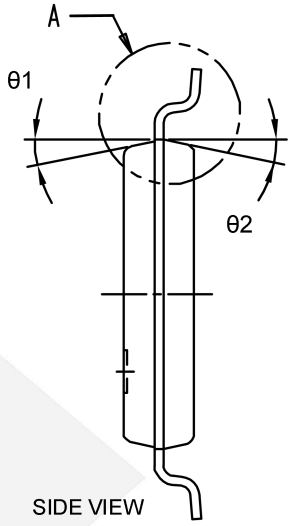
15. Physical Dimensions

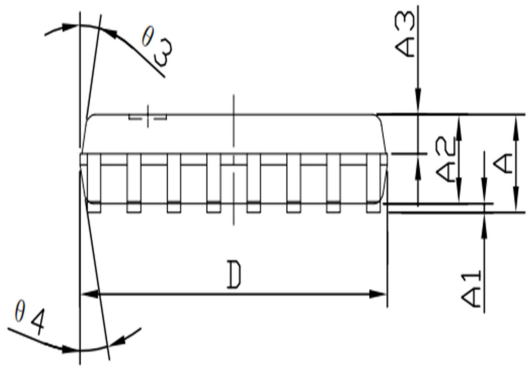
15.1. TSSOP16



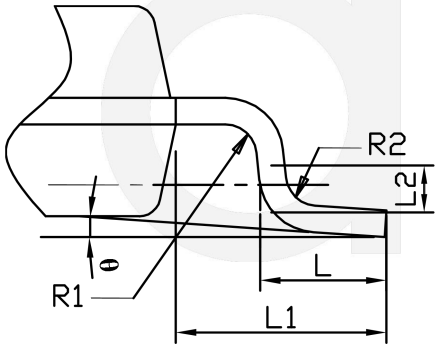
TOP VIEW



SIDE VIEW



SIDE VIEW



DETATL-A

Common Dimensions (Units of Measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	-	-	1.200
A1	0.050	0.100	0.150
A2	0.965	1.000	1.035
A3	0.415	0.440	0.465
b	0.200	-	0.280
D	4.920	5.020	5.120
E	6.200	6.400	6.60
E1	4.300	4.400	4.50
e		0.650 BSC	
L	0.45	0.60	0.75
L1		1.000 REF 4.50	
L2		0.250 BSC	
R1		0.150 REF	
R2		0.150 REF	
θ	0°	-	8°
θ1 ~ θ4		12° REF 12° 14°	

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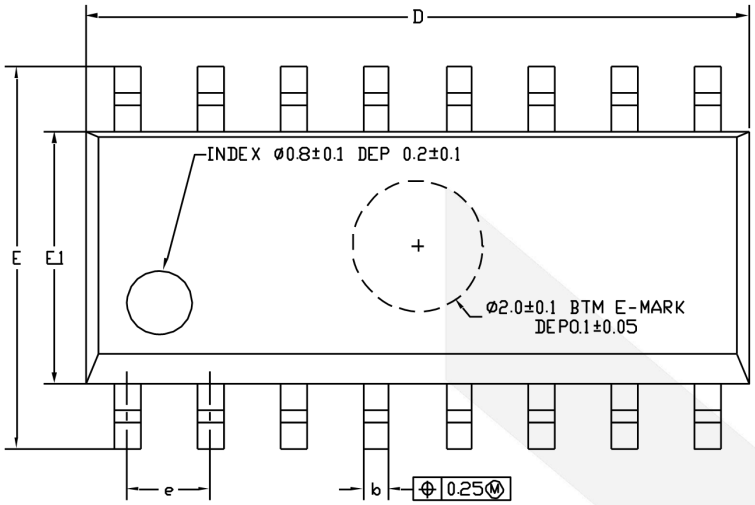
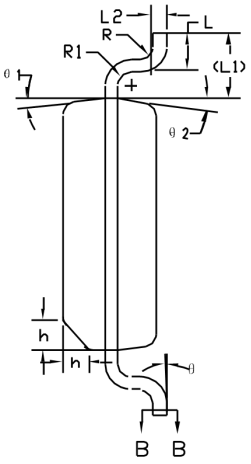
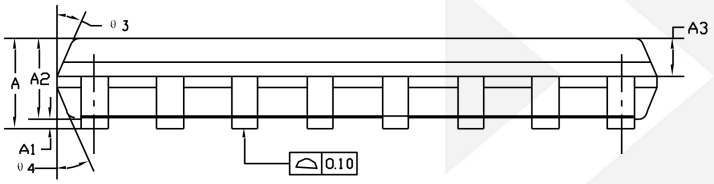
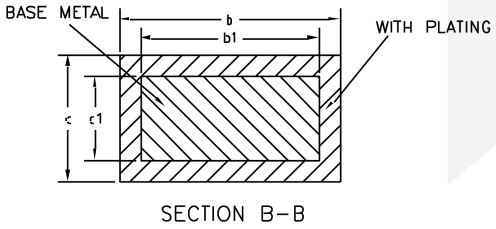
15.2. SOP16









SECTION B–B

Common Dimensions (Units of Measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36	-	0.51
b1	0.35	0.40	0.45
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	9.80	9.90	10.06
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	-	-
R1	0.07	-	-
h	0.30	0.40	0.50
θ	0°		8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

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