DIO74548

Low-Voltage, 8-Channel I²C Switch with Reset

Description

The DIO74548 is an 8-channel, bidirectional translating switch that can be controlled through the I²C bus. The SCL/SDA upstream signal pair fans out to eight downstream pairs, or channels. The contents of the programmable control register determine the pair or pairs of SCn/SDn to be selected. The downstream channels resolve the I²C slave address conflicts.

Either asserting the $\overline{\text{RESET}}$ pin low or cycling the power supply, which is called power-on reset (POR), resets the state machine of the device and deselect all channels if one of the downstream I²C buses get stuck in a low state.

The voltage conversion feature enables parts of 1.8 V, 2.5 V, or 3.3 V to communicate with 5 V parts without any additional protection by using external pull-up resistors to pull the bus to the desired voltage level for each channel. All I/O pins have a 5 V tolerance.

Features

- 1-to-8 bidirectional translating switches
- I²C bus and SMBus compatible
- Active-low reset input
- Three address pins, allowing up to eight DIO74548 devices on the I²C bus
- Channel selection through an I²C bus, in any combination
- Power up with all switch channels deselected
- Low R_{ON} switches
- Allows voltage-level translation between 1.8 V, 2.5 V, 3.3 V, and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power-supply voltage range: 1.65 V to 5.5 V
- Input tolerance: 5 V
- Clock frequency: 0 to 400 kHz
- ESD HBM ±8000 V
- ESD CDM ±2000 V
- Package: TSSOP24 and QFN4*4-24

Applications

- Servers
- Routers (telecom switching equipment)
- Factory automation
- Products with I²C slave address conflicts

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Ordering Information

Part Number	Top Marking	RoHS	T_A	Package	
DIO74548CT24	DGDE4H	Green	-40 to +125°C	TSSOP24	Tape & Reel, 2500
DIO74548CN24	DGDE4H	Green	-40 to +125°C	QFN4*4-24	Tape & Reel, 5000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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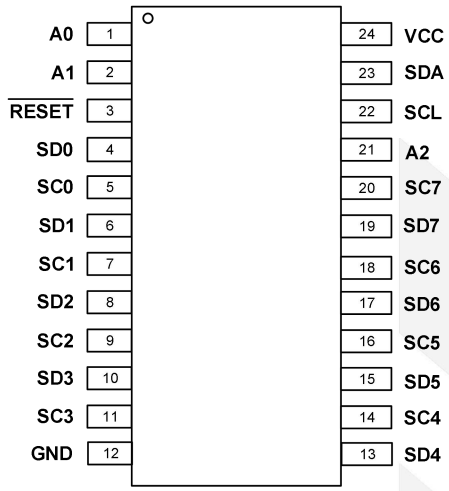
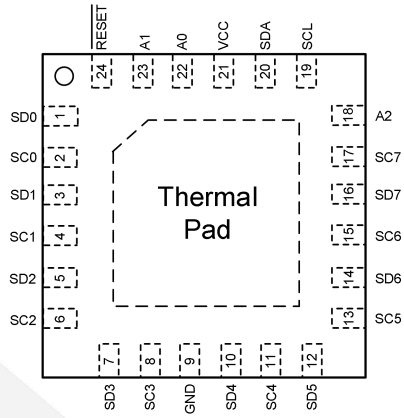
1. Pin Assignment and Functions



TSSOP24

Top view



QFN4*4-24

Top view

Pin			I/O	Description
Name	TSSOP24	QFN4*4-24		
A0	1	22	I	Address input 0. Connect directly to V_{CC} or ground
A1	2	23	I	Address input 1. Connect directly to V_{CC} or ground
A2	21	18	I	Address input 2. Connect directly to V_{CC} or ground
GND	12	9	-	Ground
$\overline{\text{RESET}}$	3	24	I	Active-low reset input. Connect to V_{CC} or V_{DPUM}(1) through a pull-up resistor, if not used.
SD0	4	1	I/O	Serial data 0. Connect to V_{DPU0} through a pull-up resistor
SC0	5	2	I/O	Serial clock 0. Connect to V_{DPU0} through a pull-up resistor
SD1	6	3	I/O	Serial data 1. Connect to V_{DPU1} through a pull-up resistor
SC1	7	4	I/O	Serial clock 1. Connect to V_{DPU1} through a pull-up resistor
SD2	8	5	I/O	Serial data 2. Connect to V_{DPU2} through a pull-up resistor
SC2	9	6	I/O	Serial clock 2. Connect to V_{DPU2} through a pull-up resistor
SD3	10	7	I/O	Serial data 3. Connect to V_{DPU3} through a pull-up resistor
SC3	11	8	I/O	Serial clock 3. Connect to V_{DPU3} through a pull-up resistor
SD4	13	10	I/O	Serial data 4. Connect to V_{DPU4} through a pull-up resistor
SC4	14	11	I/O	Serial clock 4. Connect to V_{DPU4} through a pull-up resistor
SD5	15	12	I/O	Serial data 5. Connect to V_{DPU5} through a pull-up resistor
SC5	16	13	I/O	Serial clock 5. Connect to V_{DPU5} through a pull-up resistor

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SD6	17	14	I/O	Serial data 6. Connect to V_{DPU6} through a pull-up resistor
SC6	18	15	I/O	Serial clock 6. Connect to V_{DPU6} through a pull-up resistor
SD7	19	16	I/O	Serial data 7. Connect to V_{DPU7} through a pull-up resistor
SC7	20	17	I/O	Serial clock 7. Connect to V_{DPU7} through a pull-up resistor
SCL	22	19	I/O	Serial clock bus. Connect to V_{DPUM} through a pull-up resistor
SDA	23	20	I/O	Serial data bus. Connect to V_{DPUM} through a pull-up resistor
VCC	24	21	Power	Supply voltage

Note:

(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C reference voltage and V_{DPU0} - V_{DPU7} are theslave channel reference voltages.

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2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		-0.5	7	V
V_{IN}	Input voltage		-0.5	7	V
I_{IN}	Input current		-20	20	mA
I_{OUT}	Output current		-25		mA
I_{CC}	Supply current		-100	100	mA
T_{STG}	Storage temperature		-65	150	°C
T_J	Max junction temperature	$V_{CC} \leq 3.6$ V		130	°C
		$V_{CC} \leq 5.5$ V		90	

3. Recommended Operating Condition

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage	-40°C ≤ T_A ≤ 85°C	1.65	5.5	V
		85°C < T_A ≤ 125°C	1.65	3.6	
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	6	V
		A2-A0, $\overline{\text{RESET}}$	0.7 × V_{CC}	V_{CC} + 0.5	
V_{IL}	Low-level input voltage	SCL, SDA	-0.5	0.3 × V_{CC}	V
		A2-A0, $\overline{\text{RESET}}$	-0.5	0.3 × V_{CC}	
T_A	Operating free-air temperature	3.6 V < V_{CC} ≤ 5.5 V	-40	85	°C
		1.65 V ≤ V_{CC} ≤ 3.6 V	-40	125	

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4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
ESD	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±8000	V
	Charged-device model (CDM), per JEDEC specification JS-002	±2000	

5. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Metric	DIO74548		Unit
		TSSOP24	QFN4*4-24	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109	57	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	63	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63	34	°C/W

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6. Electrical Characteristics

The values are obtained under these conditions unless otherwise specified: V_{CC} = 1.65 V to 5.5 V, typical values are at nominal supply voltage, T_A = 25°C.

Symbol	Parameter	Test Conditions	V_{CC}	Min	Typ	Max	Unit
V_{PORR}	Power-on reset voltage, V_{CC} rising	No load, V_I = V_{CC} or GND(1)			1.3	1.55	V
V_{PORF}	Power-on reset voltage, V_{CC} falling(2)	No load, V_I = V_{CC} or GND(1)		0.85	1.1		V
V_{pass}	Switch output voltage	$V_{IN(sw)}$ = V_{CC}, I_{SWout} = -100 µA	5 V		3.5		V
			4.5 V to 5.5 V	2.9		4	
			3.3 V		2		
			3 V to 3.6 V	1.6		2.5	
			2.5 V		1.4		
			2.3 V to 2.7 V	1.1		2	
			1.8 V		0.8		
			1.65 V to 1.95 V	0.5		1.2	
I_{OL}	SDA	V_{OL} = 0.4 V	1.65 V to 5.5 V	3	15		mA
		V_{OL} = 0.6 V		6	20		
I_{IN}	SCL, SDA	V_{IN} = V_{CC} or GND(1)	1.65 V to 5.5 V	-1		1	µA
	SC7-SC0, SD7-SD0			-1		1	
	A2-A0			-1		1	
	$\overline{RESET}$			-1		1	
I_{CC}	Operating mode	V_{IN} = V_{CC} or GND(1), I_{OUT} = 0, f_{SCL} = 400 kHz	5.5 V		50		µA
			3.6 V		21		
			2.7 V		19		
			1.65 V		10		
		V_I = V_{CC} or GND(1), I_{OUT} = 0, f_{SCL} = 100 kHz	5.5 V		4		
			3.6 V		2		
			2.7 V		1.5		
			1.65 V		1		
	Standby mode	V_{IN} = GND(1), I_{OUT} = 0, -40°C ≤ T_A ≤ 85°C, Low inputs	5.5 V		0.45	2	
			3.6 V		0.3	2	
			2.7 V		0.22	1	

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			1.65 V		0.13	1	
		V_{IN} = V_{CC}, I_{OUT} = 0, -40°C ≤ T_A ≤ 85°C, High inputs	5.5 V		0.45	2	
			3.6 V		0.3	2	
			2.7 V		0.22	1	
			1.65 V		0.13	1	
		V_{IN} = V_{CC} or GND, I_{OUT} = 0, 85°C < T_A ≤ 125°C, Low and high inputs	3.6 V		0.54	2	
			2.7 V		0.45	1.5	
			1.65 V		0.31	1	
ΔI_{CC}	Supply-currentchange SCL, SDA	SCL or SDA input at 0.6 V, other inputs at V_{CC} or GND(1)	1.65 V to 5.5 V		3	20	μA
		SCL or SDA input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND			3	20	
C_{IN}	A2-A0	V_{IN} = V_{CC} or GND(1)	1.65 V to 5.5 V		4		pF
	$\overline{RESET}$				4		
	SCL	V_{IN} = V_{CC} or GND(1), switch off			20		
$C_{IO(OFF)}$ (3)	SDA	V_{IN} = V_{CC} or GND(1), switch off	1.65 V to 5.5 V		20		pF
	SC7-SC0, SD7-SD0				5.5		pF
R_{ON}	Switch-on resistance	V_{OUT} = 0.4 V, I_{OUT} = 15 mA	4.5 V to 5.5 V	2.5	4.5	7	Ω
			3 V to 3.6 V	3	6	10	
		V_{OUT} = 0.4 V, I_{OUT} = 10 mA	2.3 V to 2.7 V	4	8	12	
			1.65 V to 1.95 V	6.5	16	25	

Note:

(1) $\overline{RESET}$ = V_{CC} (held high) when all other input voltages, V_{IN} = GND.

(2) The power-on reset circuit resets the I^2C bus logic with V_{CC} < V_{PORF}.

(3) $C_{IO(ON)}$ depends on internal capacitance and external capacitance added to the SCn lines when channel(s) are ON.

(4) Specifications subject to change without notice.

7. Reset Timing Requirements

Over recommended operating free-air temperature range (unless otherwise noted).

Symbol	Parameter		Min	Max	Unit
$t_{W(L)}$(1)	Pulse duration, $\overline{RESET}$ low	V_{CC} ≥ 2.5 V	18		ns
		1.65 V ≤ V_{CC} < 2.5 V	28		
$t_{REC(STA)}$(1)	Recovery time from $\overline{RESET}$ to start		0		

Note:

(1) Guaranteed by design.

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8. Switching Characteristics

Over recommended operating free-air temperature range, $C_L \leq 100$ pF unless otherwise noted .

Symbol	Parameter		From (input)	To (output)	Min	Typ	Max	Unit
t_{pd} (1)	Propagation delay time	R_{ON} = 16 Ω, C_L = 15 pF	SDA or SCL	SDn or SCn		0.24		ns
		R_{ON} = 16 Ω, C_L = 50 pF				0.8		
t_{rst}(2)(3)	$\overline{\text{RESET}}$ time (SDA clear)		$\overline{\text{RESET}}$	SDA			500	ns

Note:

(1) The propagation delay is the calculated RC time constant of the typical switch on-state resistance and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(2) t_{rst} is the propagation delay measured from the time the $\overline{\text{RESET}}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of $t_{W(L)}$.

(3) Guaranteed by design.

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9. Typical Performance Characteristics

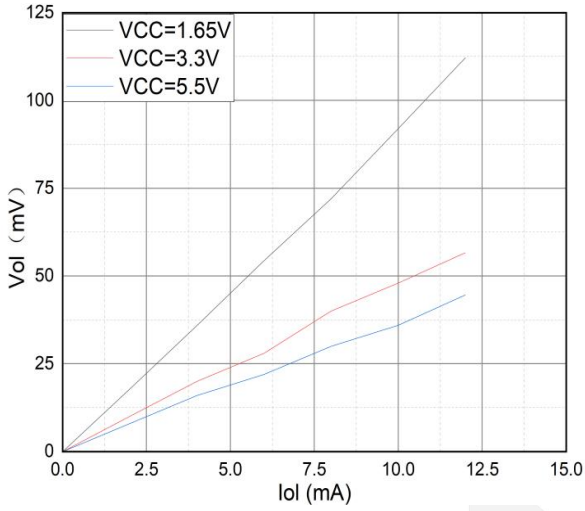

Figure 1. SDA output low voltage vs. Load current

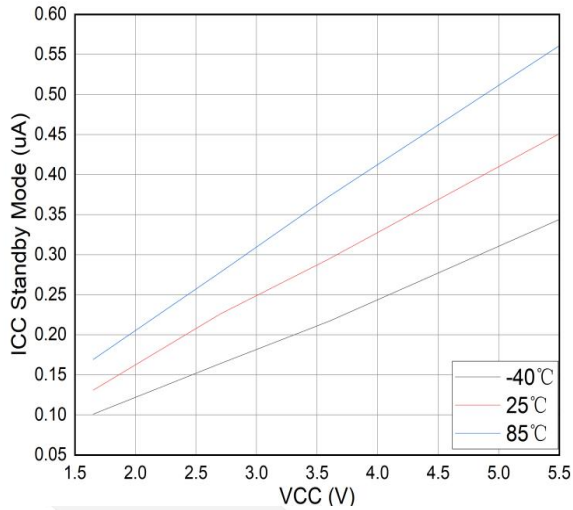

Figure 2. Standby current vs. Supply voltage

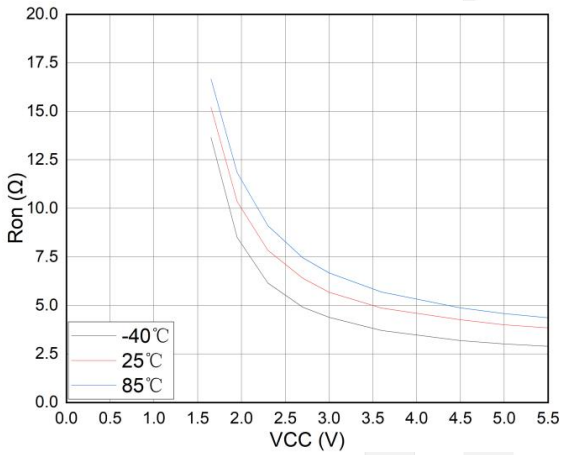

Figure 3. On-resistance vs. Supply voltage

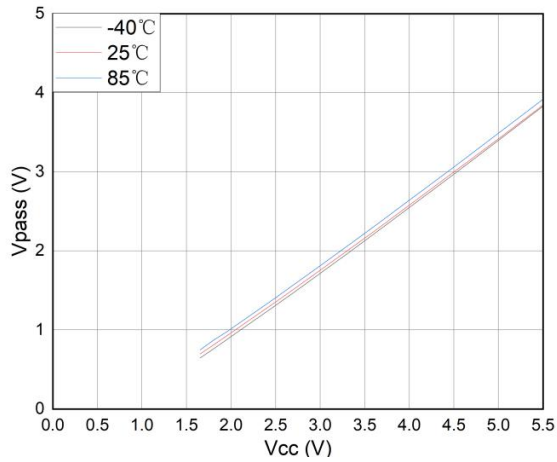

Figure 4. Pass-gate voltage vs. Supply voltage

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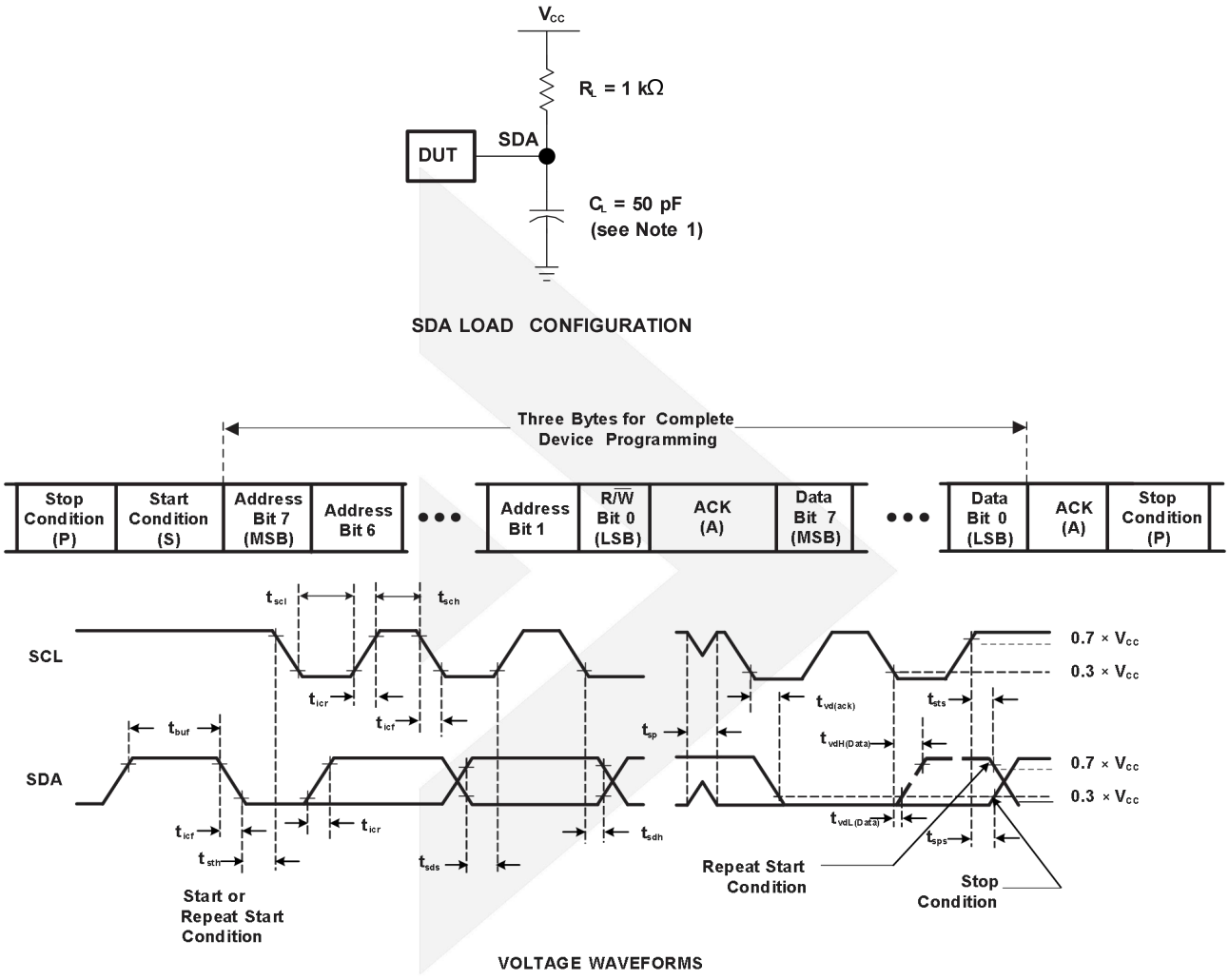
10. Parameter Measurement Information



Note:

(1) C_L includes probe and jig capacitance.

(2) All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

(3) Not all parameters and waveforms are applicable to all devices.

Figure 5. I^2C load circuit and voltage waveforms

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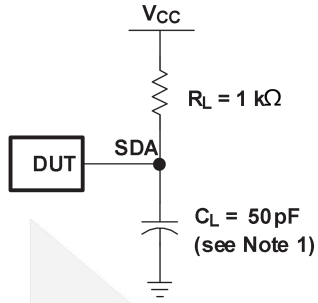
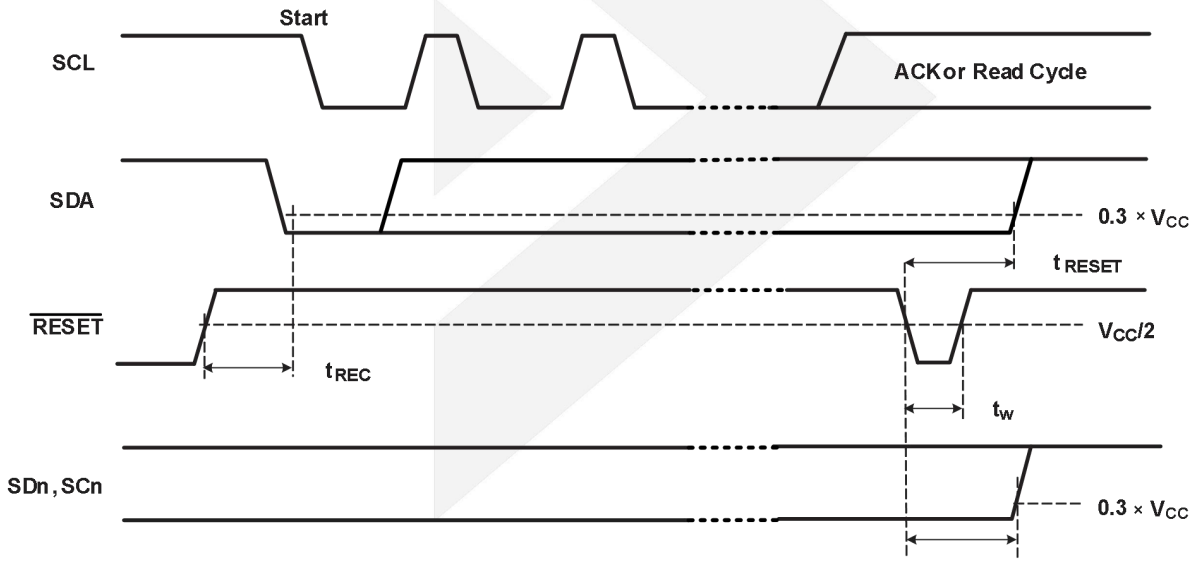


SDA LOAD CONFIGURATION



Note:

(1) C_L includes probe and jig capacitance.

(2) All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

(3) I/Os are configured as inputs.

(4) Not all parameters and waveforms are applicable to all devices.

Figure 6. Reset load circuit and voltage waveforms

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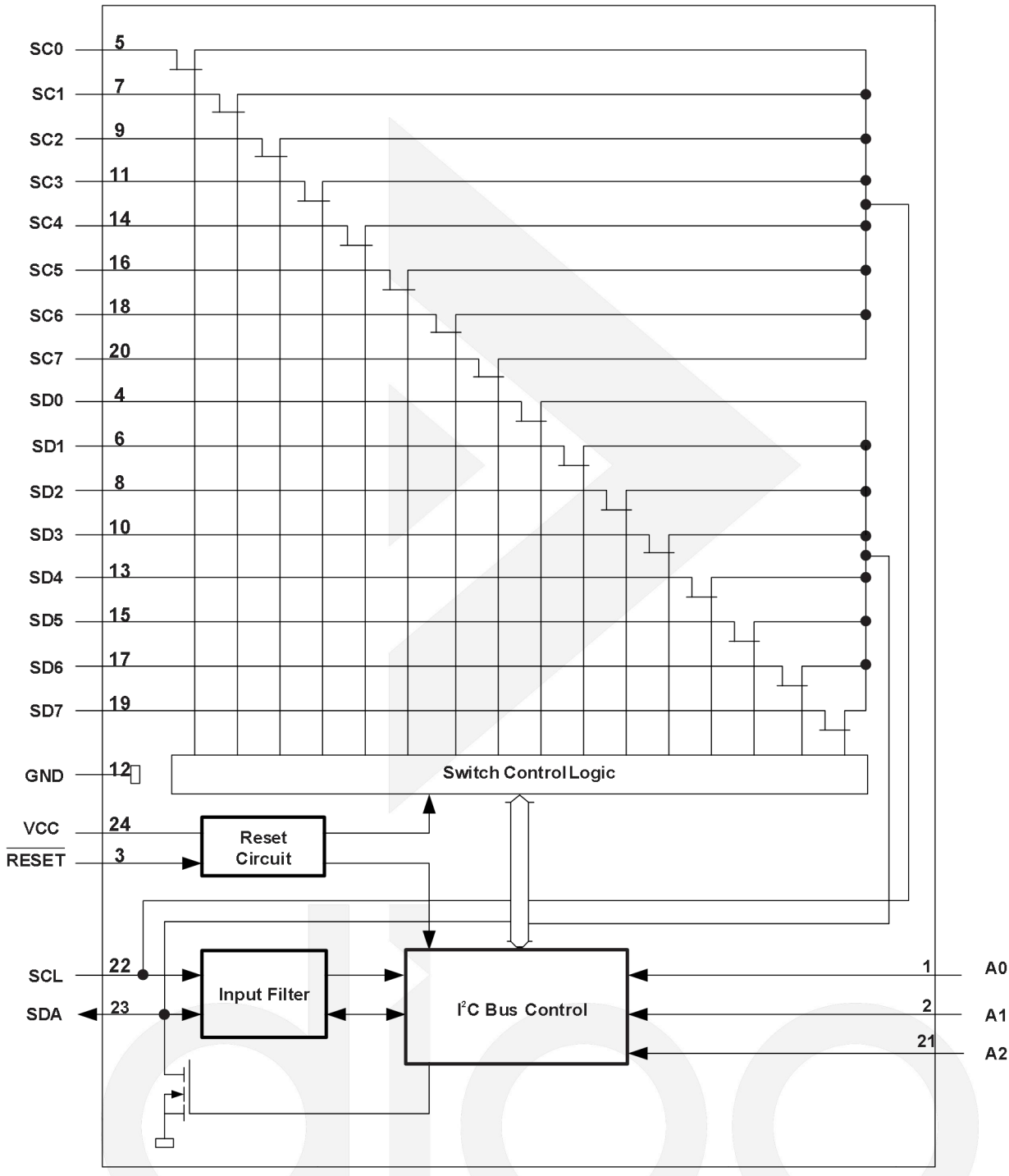
11. Block Diagram



Note:

(1) Pin numbers are for the TSSOP24 package.

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12. Function Description

The DIO74548 is an 8-channel, bidirectional translating switch that can be controlled through the I^2C bus. The SCL/SDA upstream signal pair fans out to eight downstream pairs, or channels. The contents of the programmable control register determine the pair or pairs of SCn/SDn to be selected. The downstream channels resolve the I^2C slave address conflicts.

Either asserting the $\overline{\text{RESET}}$ pin low or cycling the power supply, which is called power-on reset (PoR) resets the state machine of the device and deselect all channels if one of the downstream I^2C buses get stuck in a low state.

The I^2C master device that is switched to communicate with several I^2C slaves controls the connections of the I^2C data path. A single 8-bit control register is written to or read from to determine the selected channels after the successful acknowledgment of the slave address which can be controlled by using a hardware to select A0, A1, and A2 pins.

The voltage conversion feature enables parts of 1.8 V, 2.5 V, or 3.3 V to communicate with 5 V parts without any additional protection by using external pull-up resistors to pull the bus to the desired voltage level for each channel. All I/O pins have a 5 V tolerance.

12.1. Device functional modes

12.1.1. $\overline{\text{RESET}}$ input

The $\overline{\text{RESET}}$ input is an active-low signal. If a bus-fault condition occurs, reset the register and I^2C state machine and deselect all channels by asserting the signal low for at least a pulse duration. Connect the pin to VCC by using a pull-up resistor.

12.1.2. Power-on reset

A power-on reset results from cycling power to the device. When V_{CC} reaches V_{PORR}, the device enters reset condition in which the registers and I^2C state machines are initialized and all channels are deselected. Thereafter, lower V_{CC} below V_{PORF} to reset the device.

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12.2. Programming

12.2.1. I²C interface

The I²C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). The device that controls the message is the master and the devices that are controlled by the master device are the slaves. The standard bidirectional I²C interface in the device enables configuring and reading the status of the DIO74548 by a master device. Each slave on the I²C bus has a specific device address to differentiate it from other slave devices on the same I²C bus.

The bus is idle when both SDA and SCL lines are high after a STOP condition (see Figure 7 and Figure 8). Data transfer might be initiated when the bus is idle.

This is how a master access a slave device:

- If a master wants to send data to a slave:
  1. Master-transmitter sends a START condition and addresses the slave-receiver.
  2. Master-transmitter sends data to slave-receiver.
  3. Master-transmitter terminates the transfer by sending a STOP condition.

- If a master wants to receive or read data from a slave:
  1. Master-receiver sends a START condition and addresses the slave-transmitter.
  2. Master-receiver sends the requested register to read to slave-transmitter.
  3. Master-receiver receives data from the slave-transmitter.

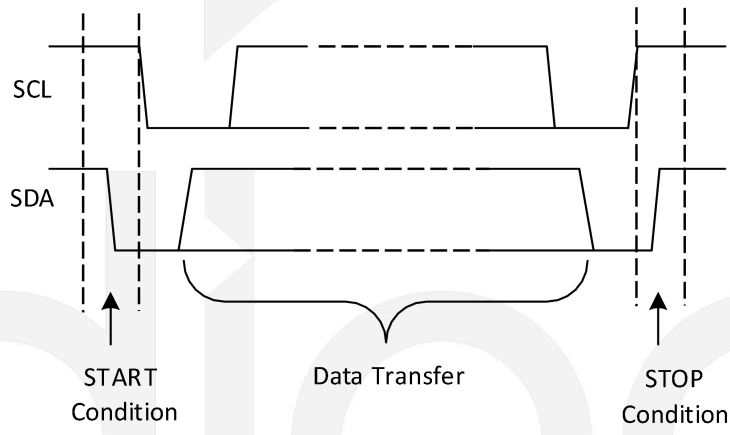

Figure 7. Definition of start and stop conditions

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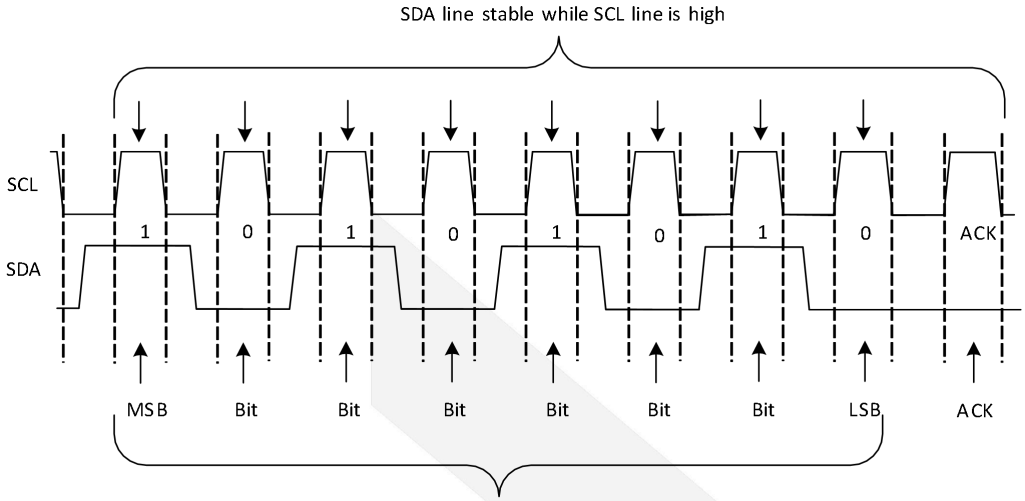

Figure 8. Bit transfer

12.2.2. Device address

Figure 9 shows the address byte of the DIO74548.

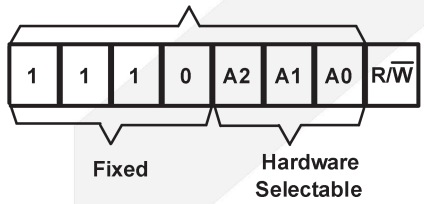

Figure 9. DIO74548 address

The last bit of the slave address defines the operation to be read or write. When the last bit is 1 or high, it means to read; when the last bit is 0 or low, it means to write. Table 1 shows the slave address reference.

Table 1. Address reference

Inputs			I²C Bus Slave Address
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

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12.2.3. Bus transactions

The DIO74548 has only one register in the device, which is why it can be written to directly by sending the register data immediately after the slave address, skipping the register number.

To write to a slave, the master sends a START condition on the bus, followed by the address of the slave and the last bit set to 0. After the slave acknowledges, the master sends the control register data to the slave and terminates the transmission with a STOP condition. The amount of bytes sent has no limit, but the register only save the last byte. Figure 10 is an example of writing a single byte to a slave register.

12.2.4. Control register

After the slave acknowledges, the bus master sends a command byte that is stored in the control register in the DIO74548. The I^2C bus can write to or read from the control register. Each bit in the command byte corresponds to a SCn/SDn channel. A high or 1 selects the channel. Select more than one channel at the same time is possible. The selected channel only becomes active after a stop condition is placed on the I^2C bus. The condition ensures that all SCn/SDn lines are in a high state when the channel is active, avoiding false conditions at the time of connection. A stop condition must follows immediately after the acknowledge cycle. The device only saves the last byte received if multiple bytes are sent to the device.

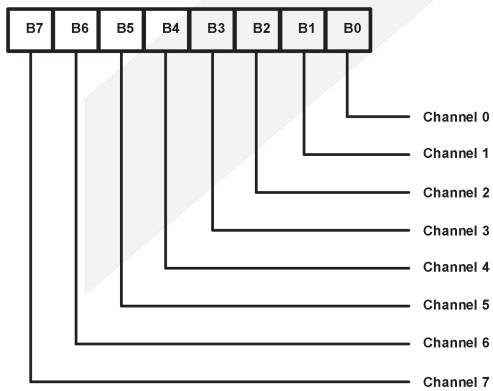

Figure 10. Control resistor

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Table 2 shows the DIO74548 command byte definition.

Table 2. Command byte definition

Control Register Bits								Command
B7	B6	B5	B4	B3	B2	B1	B0	
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
			1					Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
		1						Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
	1							Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1								Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/resetdefault state

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13. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

Applications of the DIO74548 include an I²C or SMBus master device and eight I²C salve devices. In an application where I²C slave address conflicts happen, the downstream channels can resolve the conflicts. In an application where no I²C slave address conflicts happen, connect the slave devices to any desired channel to distribute the total bus capacitance of multiple channels.

13.1. Typical application

Figure 11 shows an application of DIO74548.

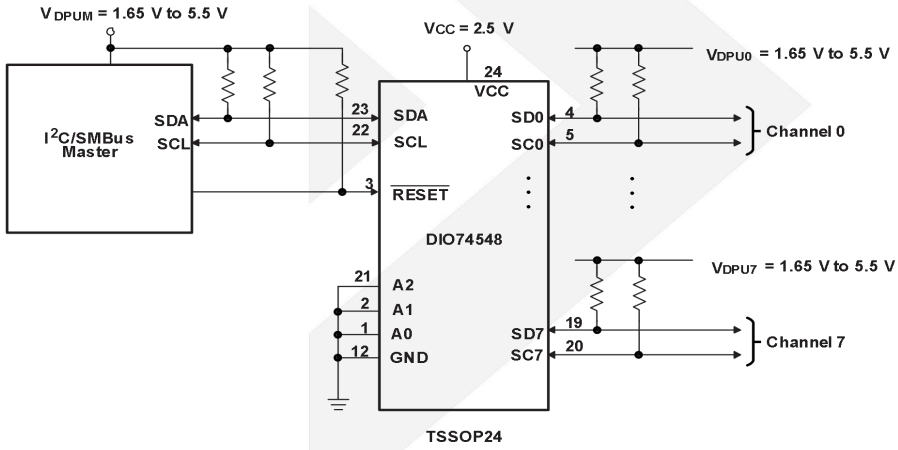

Figure 11. Typical application schematic

13.2. Design requirements

The device typically has one or more data pull-up voltages (V_{DPUX}), one for the master device (V_{DPUM}) and one for each selectable slave channel (V_{DPU0} - V_{DPU7}). V_{DPUM} and V_{DPUX} are at the same value of the supply voltage when the master device and all slave devices operates tat the same voltage.

To control the slave address of the DIO74548, use hardware to select A0, A1, and A2 pins which might be tied directly to GND or VCC.

The total I_{OL} from SCL/SDA to GND on the master side is the sum of the currents through all pull-up resistors when multiple slave channels are activated simultaneously in the application.

The device can use power supply voltage to limit the maximum voltage that is passed from one I²C bus to another due to the pass-gate construction.

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13.3. Detailed design procedure

Following the assignment of slaves to appropriate slave channels and identification of bus voltages, select the appropriate pull-up resistors for each bus. The minimum pull-up resistance can be calculated from Equation (1).

$$R_{PULL-UP(MIN)} = \frac{V_{DPUX} - V_{OL(MAX)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance can be calculated from Equation (2).

$$R_{PULL-UP(MAX)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

where

t_r is the maximum rise time (300 ns for fast-mode operation, f_{SCL} = 400 kHz

C_b is the bus capacitance.

Limit the maximum bus capacitance for an I^2C bus at or under 400 pF for fast-mode operation. The bus capacitance is almost the capacitance sum of the DIO74548, wires, connections and trances, and each individual slave on a given channel. Each of the slaves on all channels contributes to the total bus capacitance when multiple channels are active at the same time.

13.4. Application curves

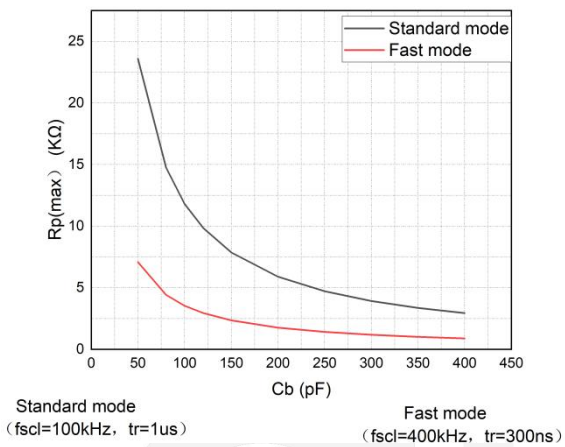
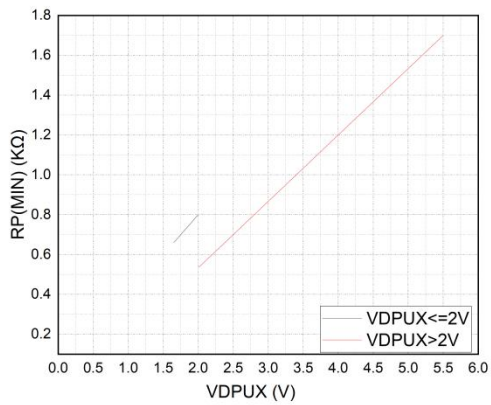


Figure 12. Maximum pull-up resistance ($R_{p(max)}$) vs. Bus capacitance (C_b)



V_{OL} = 0.2×V_{DPUX}, I_{OL} = 2 mA when V_{DPUX} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

Figure 13. Minimum Pullup Resistance ($R_{p(min)}$) vs. Pullup reference voltage (VDPUX)

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14. Power Supply Recommendations

For a successful initialization of the I2C bus logic, the power-on reset requirements must be followed when the device is powered on for the first time or whenever the device requires a power supply cycle.

The power-on reset feature can reset the DIO74548 to default conditions when a glitch or data corruption happens.The feature also is used when the device is powered on for the first time in an application. To perform the reset, cycle the power of the device as shown in Figure 14.

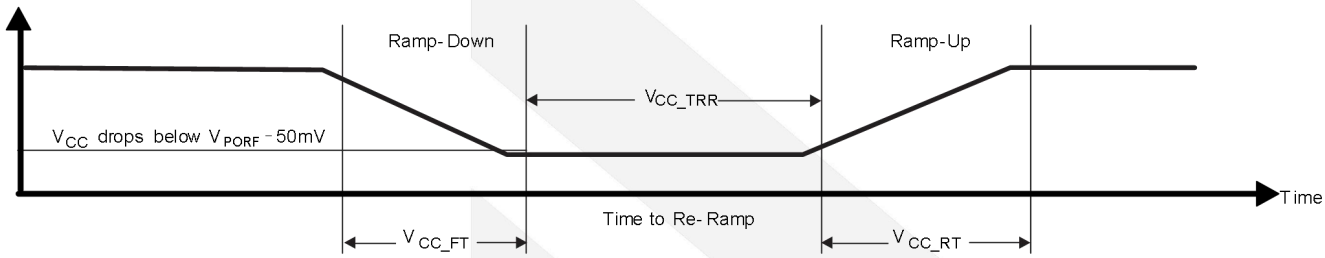

Figure 14. Power-on reset waveform

Table 3 specifies the performance of the power-on reset for DIO74548 for both types of power-on reset.

Table 3. Recommended supply sequencing and ramp rates(1)

Symbol	Parameter	Min	Max	Unit
V_{CC_FT}(2)	Fall time	1	100	ms
V_{CC_RT}(2)	Rise time	0.1	100	ms
V_{CC_TRR}(2)	Time to re-ramp (when V_{CC} drops below $V_{PORF(min)}$ - 50 mV or when V_{CC} drops to GND)	40		µs
V_{CC_GH}(3)	Level that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW} = 1 µs		1.2	V
V_{CC_GW}(3)	Glitch width that does not cause a functional disruption when V_{CC_GH} = 0.5 × V_{CC}		10	µs

Note:

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

(2) See Figure 12

(3) See Figure 13

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are interdependent. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 13 and Table 3 provide the information on how to measure these specifications.

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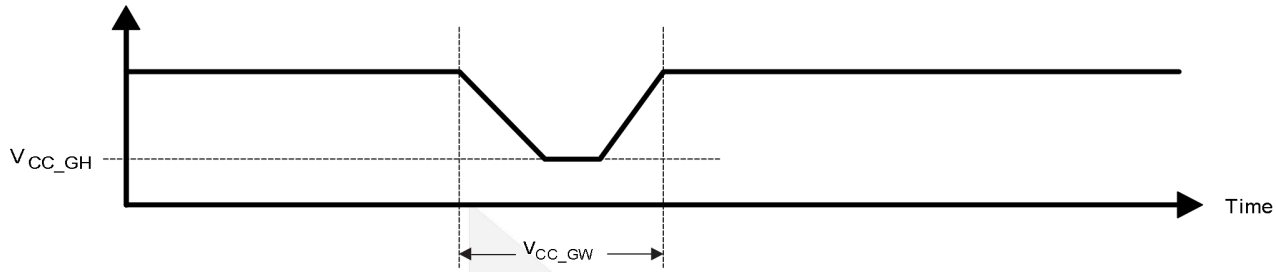

Figure 15. Glitch width and glitch height

As soon as the V_{POR} voltage level is reached, the reset condition is released and all registers and the state machine are reset to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Refer to Figure 14 and Table 3 for more information on this specification.

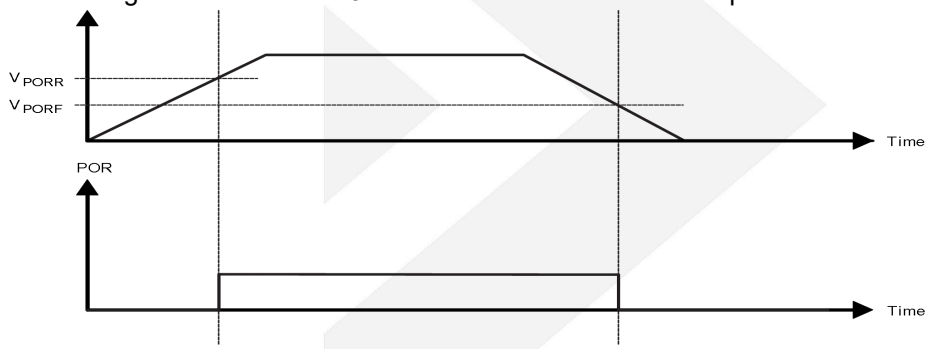

Figure 16. V_{POR}

15. Layout Guidelines

PCB layout concerns such as matched impedances and differential pairs are related to high-speed data transfer but not to I^2C signal speeds. Pins that are connected to the ground must have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias on an inner layer of the board. Use by-pass and decoupling capacitors to control the voltage on the VCC pin. Use larger capacitors to provide additional power when a short power supply glitch happens. Use a smaller capacitor to filter out high-frequency ripple.

When voltage translation is not necessary, all VDPUX voltages and VCC could be at the same potential, and all pull-up resistors could be connected to the appropriate reference voltage by a single copper plane. When voltage translation is necessary, V_{DPUM} and V_{DPU0} - V_{DPU7} might all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I^2C bus capacitance added by PCB parasitics, keep SCn and SDn as short as possible. Minimize the widths of the traces.

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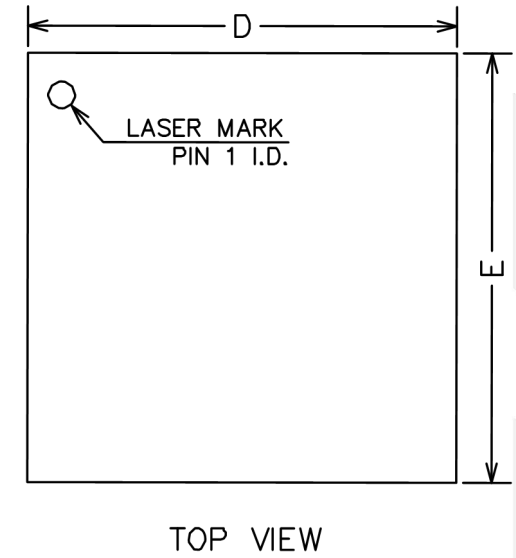
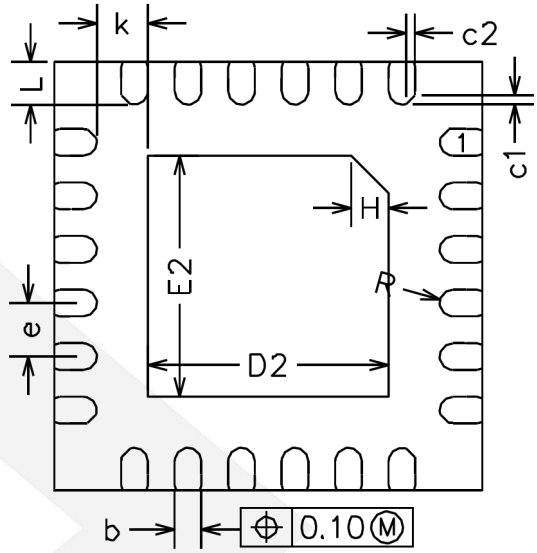
16. Physical Dimensions

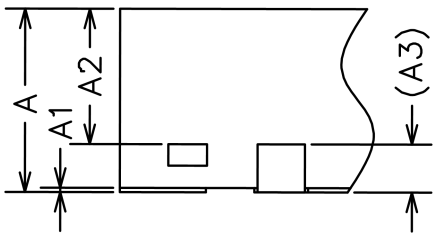
16.1. QFN4*4-24



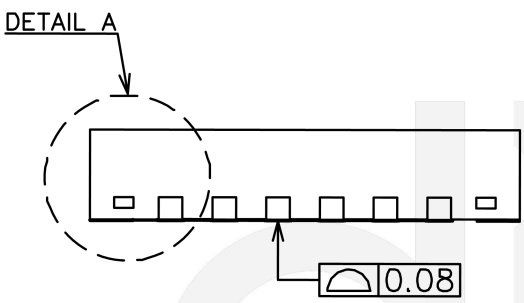
TOP VIEW



BOTTOM VIEW



DETAIL A



SIDE VIEW

Common Dimensions (Units of Measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20 REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.15	2.25	2.35
E2	2.15	2.25	2.35
e	0.40	0.50	0.60
H		0.35 REF	
K	0.30	-	-
L	0.35	0.40	0.45
R	0.09	-	-
c1	-	0.08	-
c2	-	0.08	-

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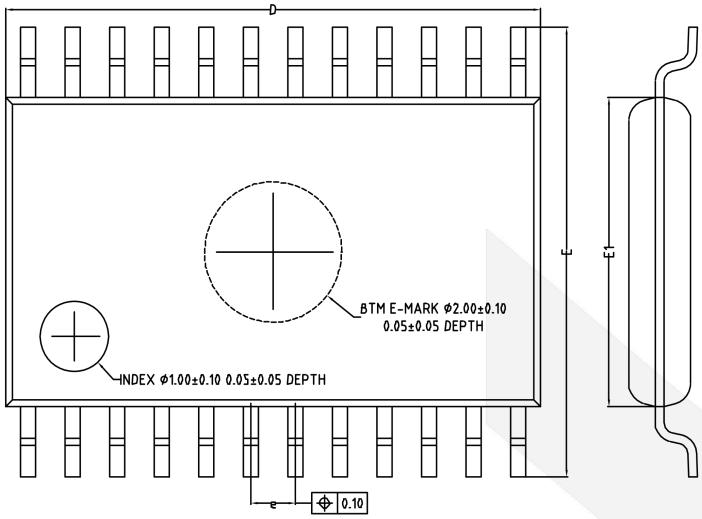
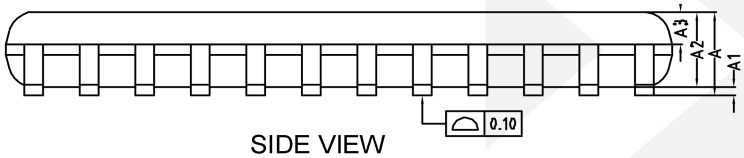
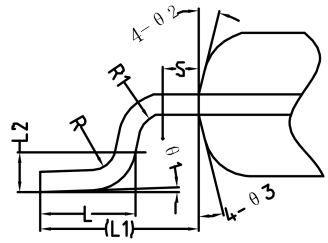
16.2. TSSOP24

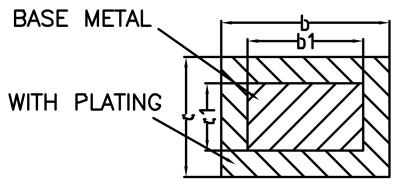


TOP VIEW



SIDE VIEW





SECTION B–B

Common Dimensions (Units of Measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	0.90	1.00
A3	0.34	0.39	0.44
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.10	-	0.19
c1	0.10	0.13	0.15
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	12°	14°	16°
θ3	12°	14°	16°

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