N and P Channel Enhancement Mode Power MOSFET

Description

This Product uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

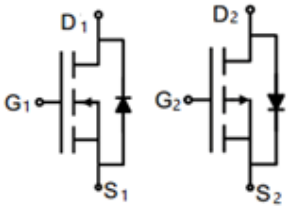
General Features

- **NMOS**
- V_{DS} 40V
- I_D (at V_{GS} = 10V) 4.5A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 41mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 68mΩ

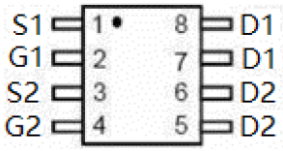
- **PMOS**
- V_{DS} -40V
- I_D (at V_{GS} = -10V) -10A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 37mΩ
- $R_{DS(ON)}$ (at V_{GS} = -4.5V) < 54mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

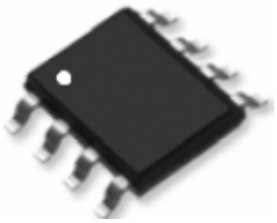
- Power switch
- DC/DC converters



Schematic diagram



Marking and pin assignment



SOP-8 Dual

Device	Package	Marking	Packaging
G05NP04S	SOP-8 Dual	G05NP04	4000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	40	-40	V
Continuous Drain Current	I_D	4.5	-10	A
Pulsed Drain Current (note1)	I_{DM}	18	-40	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Power Dissipation	P_D	2	2	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	ºC

Thermal Resistance

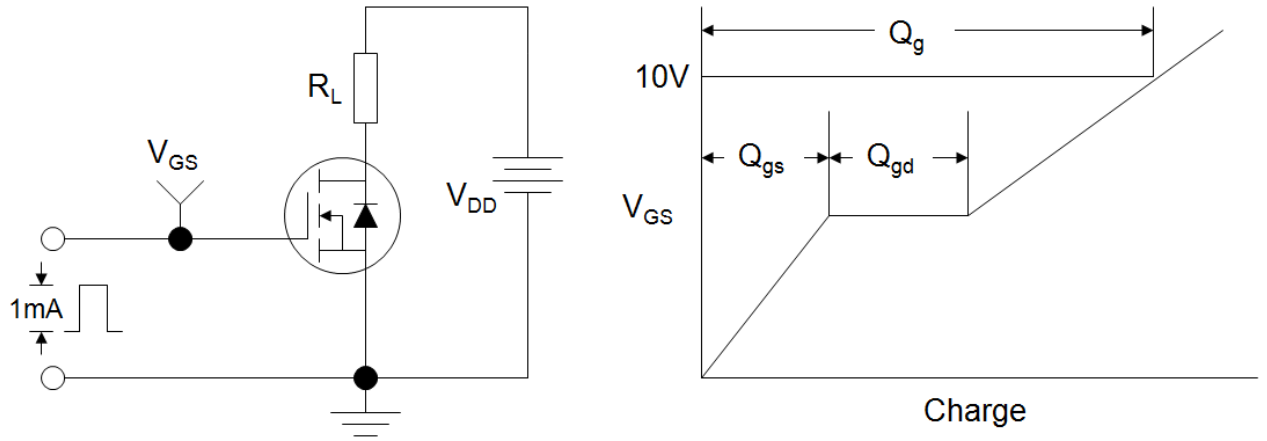
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	48	62.5	ºC/W

NMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V, T_J = 25ºC	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1	1.25	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 1A	--	27.5	41	mΩ
		V_{GS} = 4.5V, I_D = 1A	--	35	68	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=6A	--	27	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1.0MHz	--	516	--	pF
Output Capacitance	C_{oss}		--	82	--	
Reverse Transfer Capacitance	C_{rss}		--	43	--	
Total Gate Charge	Q_g	V_{DD} = 20V, I_D = 6A, V_{GS} = 10V	--	8.9	--	nC
Gate-Source Charge	Q_{gs}		--	2.4	--	
Gate-Drain Charge	Q_{gd}		--	1.4	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20V, I_D = 6A, R_G = 3Ω	--	6.4	--	ns
Turn-on Rise Time	t_r		--	3.6	--	
Turn-off Delay Time	$t_{d(off)}$		--	16.2	--	
Turn-off Fall Time	t_f		--	6.6	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	2	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 6A, V_{GS} = 0V	--	--	1.2	V

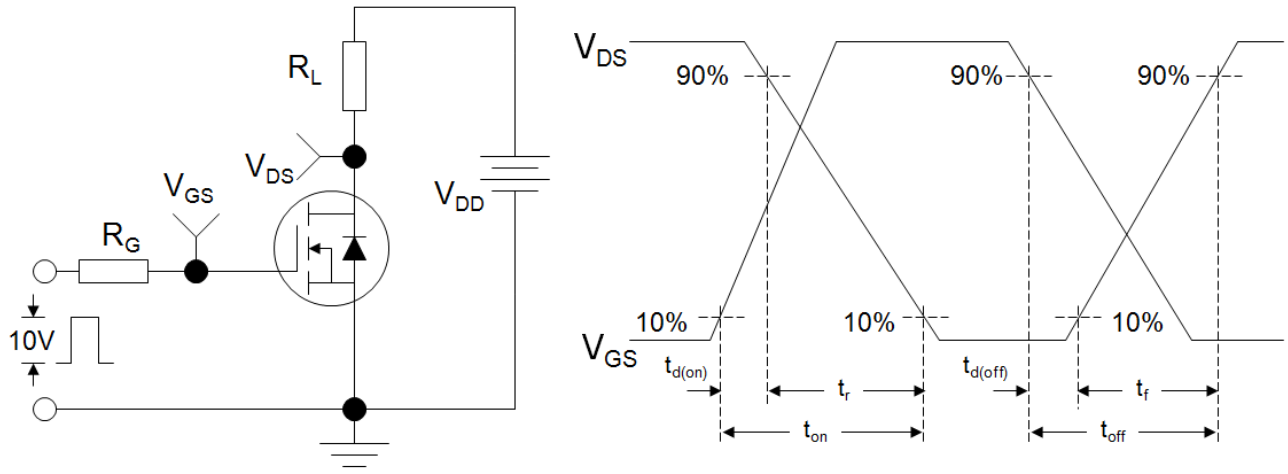
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

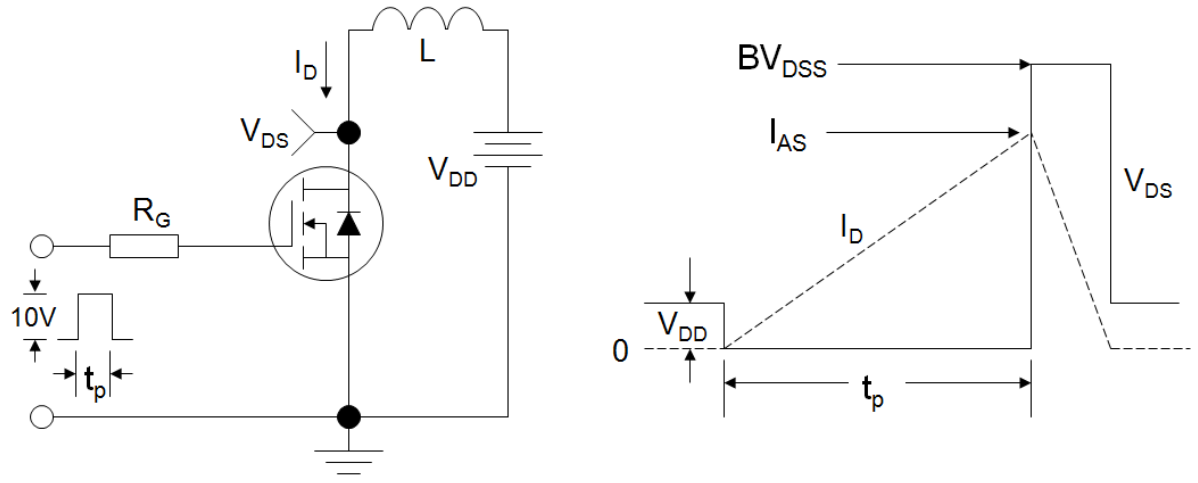
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

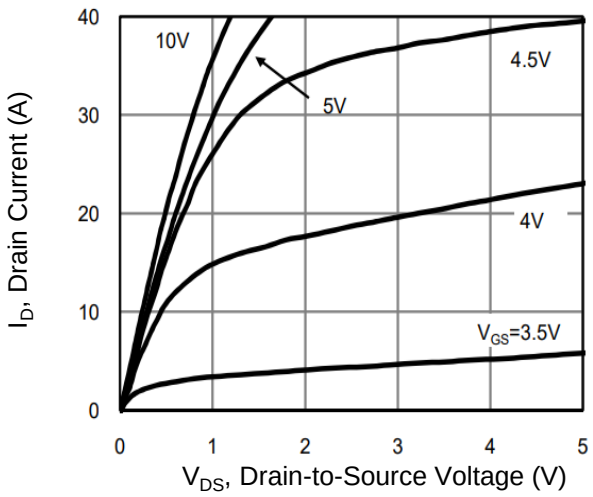


Figure 2. Transfer Characteristics

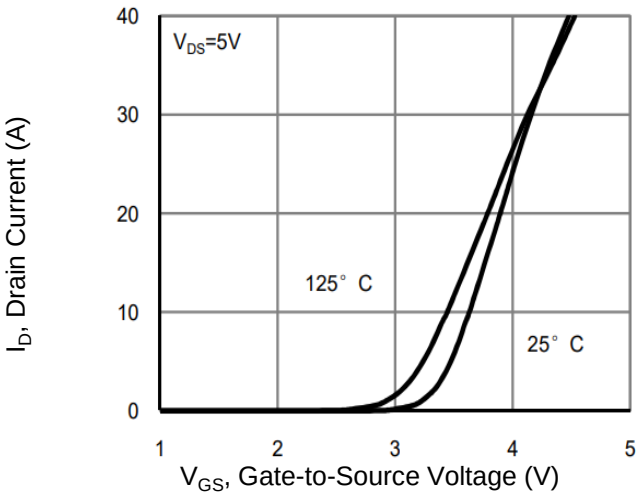


Figure 3.Drain-Source On-Resistance

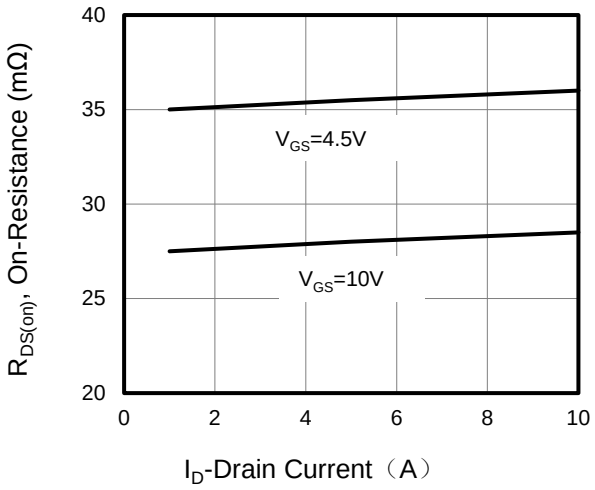


Figure 4. Gate Charge

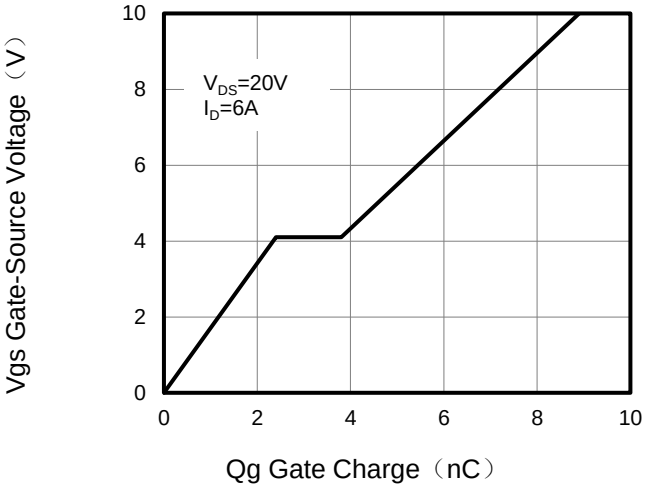


Figure 5. Capacitance

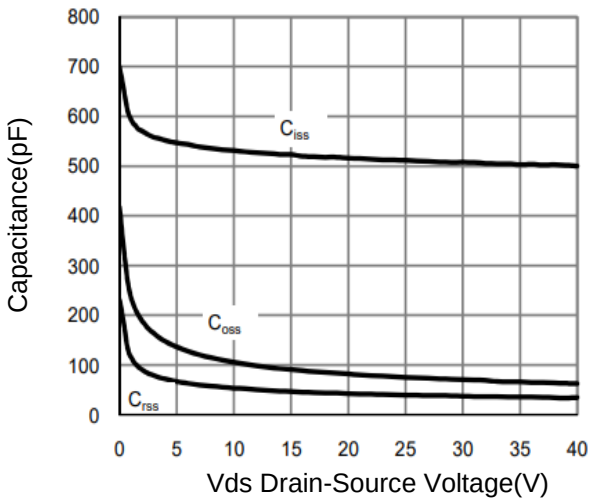
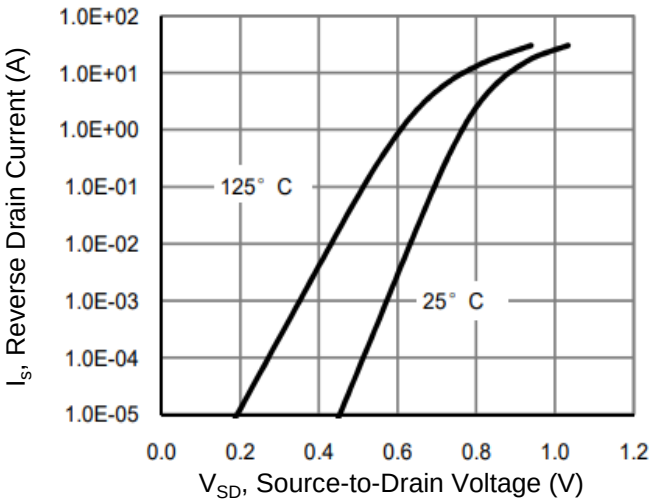


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

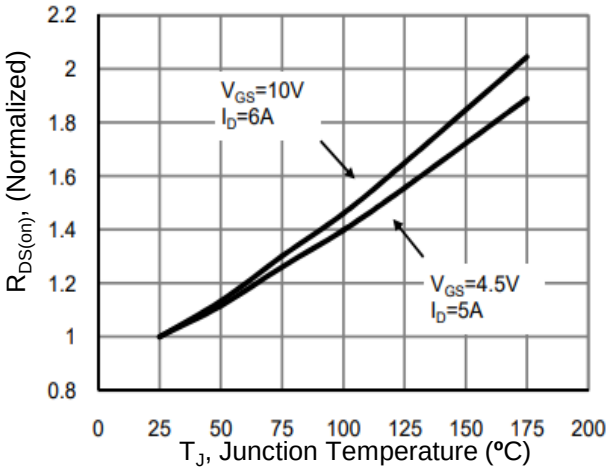


Figure 10. Safe Operation Area

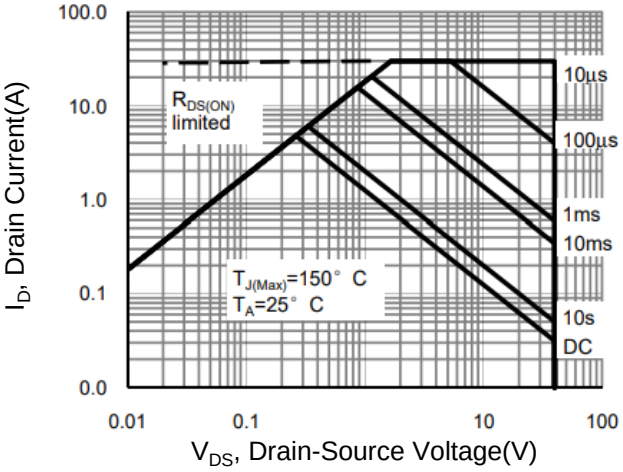
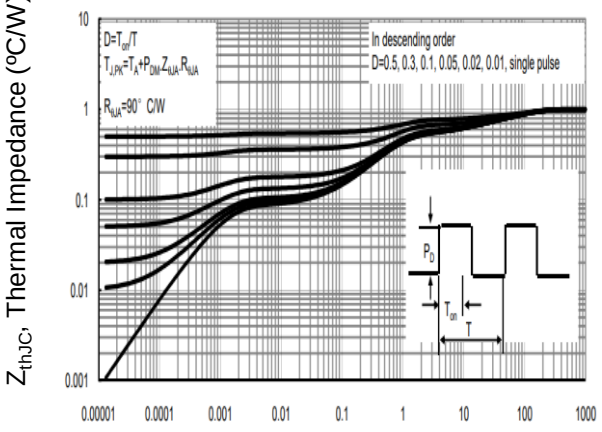


Figure 9. Normalized Maximum Transient Thermal Impedance

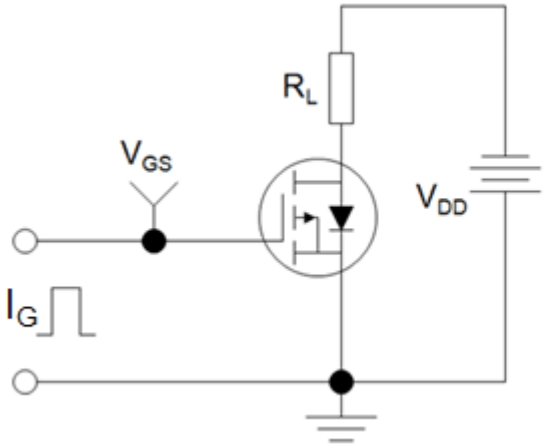


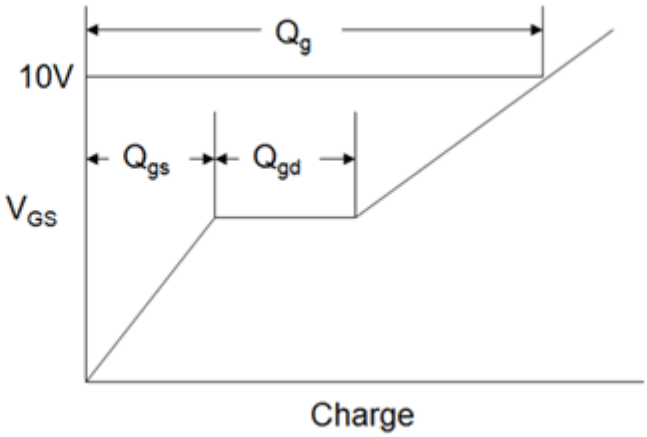
PMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V, T_J = 25ºC	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.9	-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -1A	--	26	37	mΩ
		V_{GS} = -10V, I_D = -10A	--	26	37	
		V_{GS} = -4.5V, I_D = -1A	--	28	54	
		V_{GS} = -4.5V, I_D = -10A	--	28	54	
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-8A	20	--	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -20V, f = 1.0MHz	--	520	--	pF
Output Capacitance	C_{oss}		--	100	--	
Reverse Transfer Capacitance	C_{rss}		--	65	--	
Total Gate Charge	Q_g	V_{DD} = -20V, I_D = -10A, V_{GS} = -10V	--	13	--	nC
Gate-Source Charge	Q_{gs}		--	3.8	--	
Gate-Drain Charge	Q_{gd}		--	3.1	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -20V, I_D = -10A, R_G = 6Ω	--	7.5	--	ns
Turn-on Rise Time	t_r		--	5.5	--	
Turn-off Delay Time	$t_{d(off)}$		--	19	--	
Turn-off Fall Time	t_f		--	7	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-10	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -10A, V_{GS} = 0V	--	--	-1.2	V

Notes

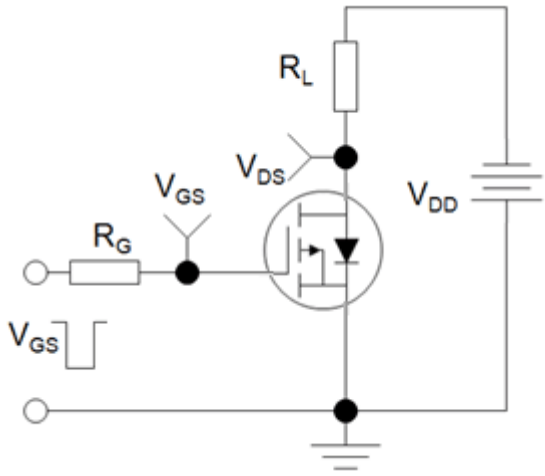
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2. Identical low side and high side switch with identical R_G

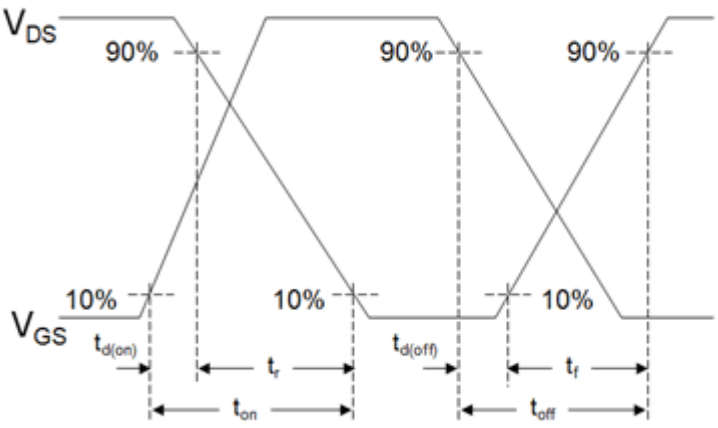
Gate Charge Test Circuit



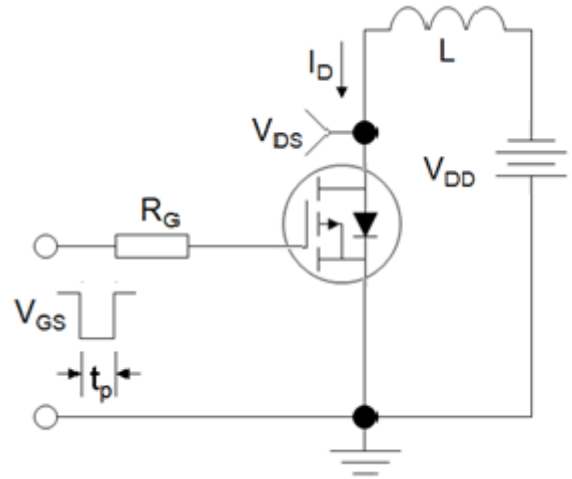


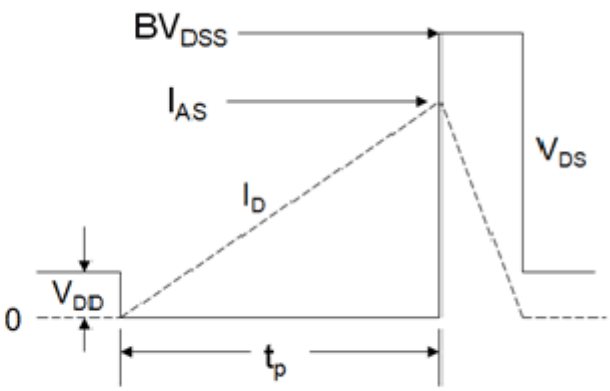
Switch Time Test Circuit





EAS Test Circuit





PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

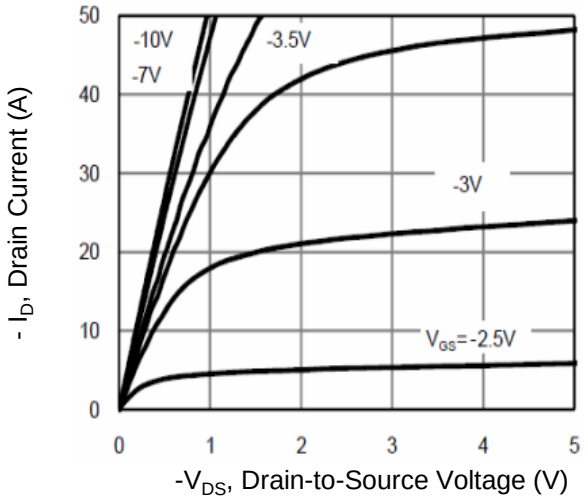


Figure 2. Transfer Characteristics

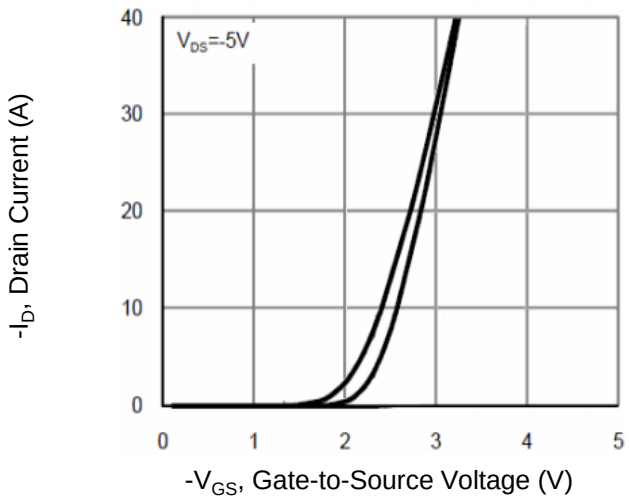


Figure 3.Rdson-Drain Current

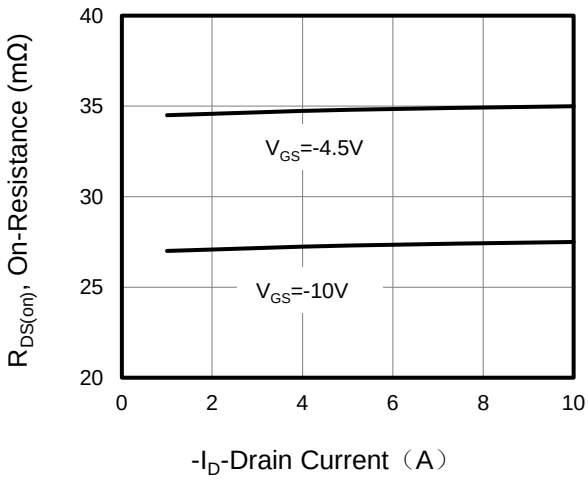


Figure 4. Gate Charge

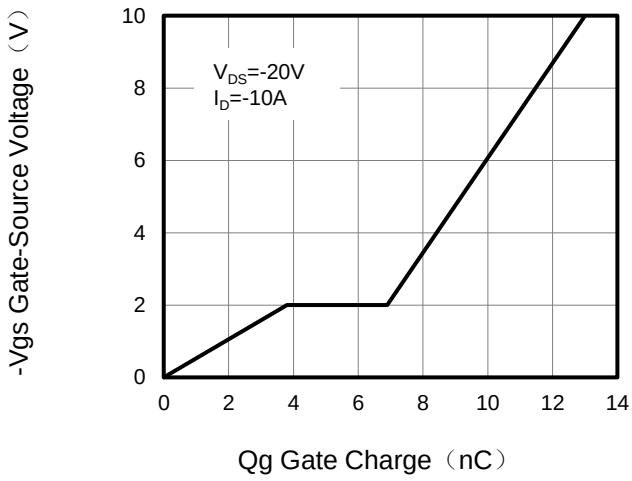


Figure 5. Capacitance

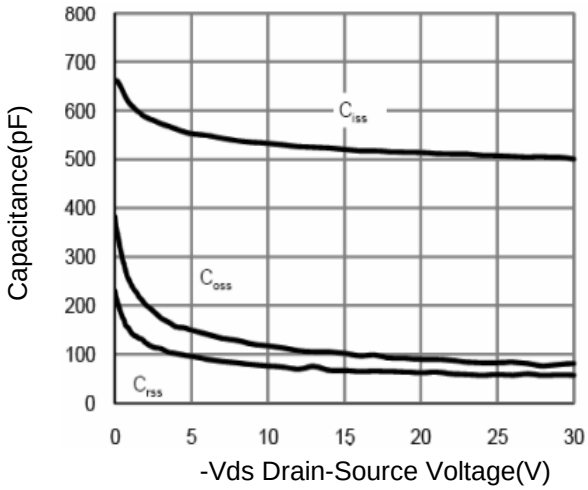
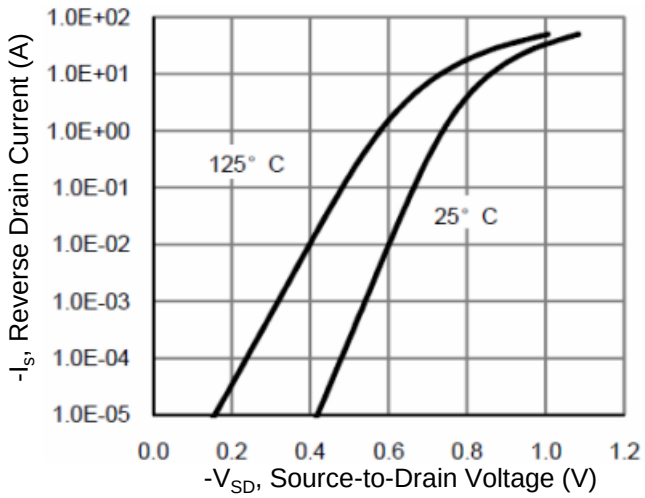


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

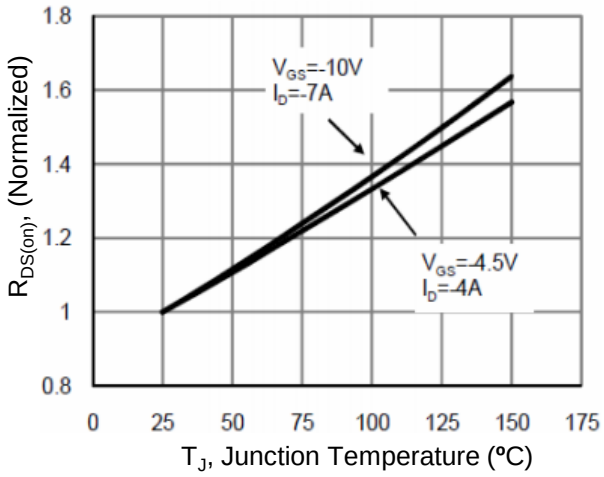


Figure 8. Safe Operation Area

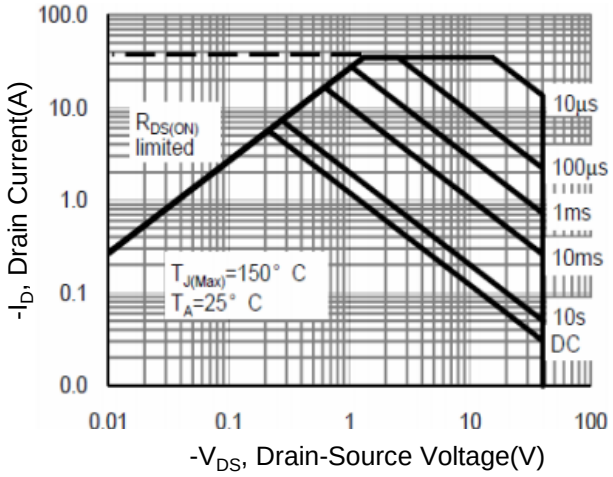
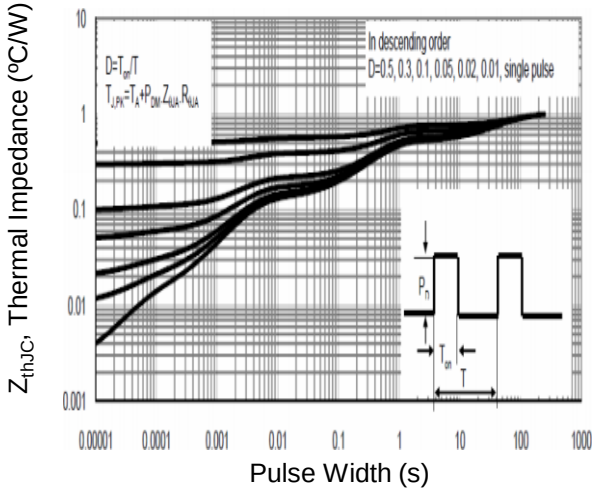
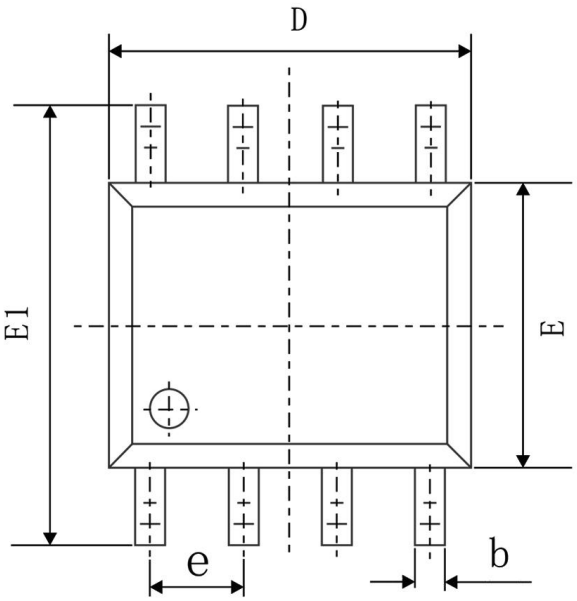


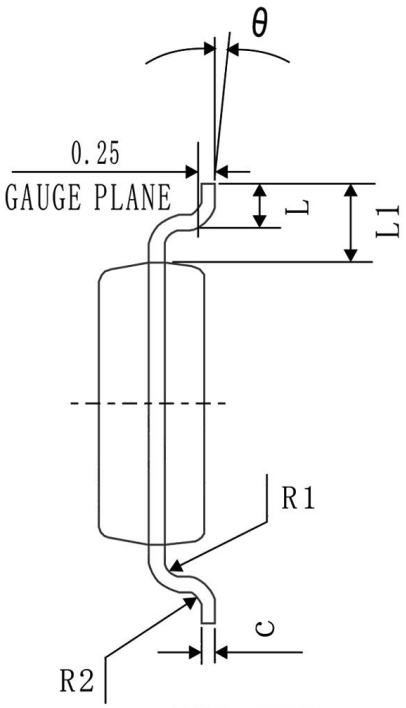
Figure 9. Normalized Maximum Transient Thermal Impedance



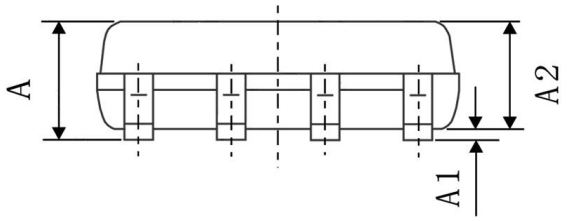
SOP-8 Dual Package Information



TOP VIEW



SIDE VIEW



SIDE VIEW

SYMBOL	MIN	NOM	MAX
A	1.40	1.60	1.80
A1	0.05	0.15	0.25
A2	1.35	1.45	1.55
b	0.30	0.40	0.50
c	0.153	0.203	0.253
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
L	0.45	0.70	1.00
θ	2°	4°	6°
L1	1.04 REF		
e	1.27 BSC		
R1	0.07 TYP		
R2	0.07 TYP		