P-Channel Enhancement Mode Power MOSFET

Description

The G7P03D2A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

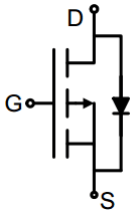
AEC-Q101 Qualified

General Features

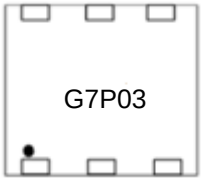
- V_{DS} -30V
- I_D (at V_{GS} = -10V) -7A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 20.5mΩ
- $R_{DS(ON)}$ (at V_{GS} = -4.5V) < 26mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

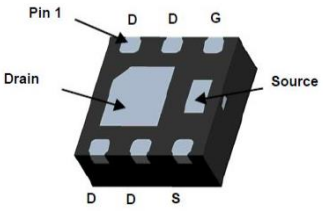
- Synchronous Rectification in SMPS or LED Driver
- UPS
- Motor Control
- BMS
- High Frequency Circuit



Schematic diagram



Marking and pin assignment



DFN2*2-6L

Device	Package	Marking	Packaging
G7P03D2A	DFN2*2-6L	G7P03	3000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	V
Continuous Drain Current	I_D	-7	A
Pulsed Drain Current (note1)	I_{DM}	-28	A
Gate-Source Voltage	V_{GS}	±20	V
Power Dissipation	P_D	1.3	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	ºC

Thermal Resistance

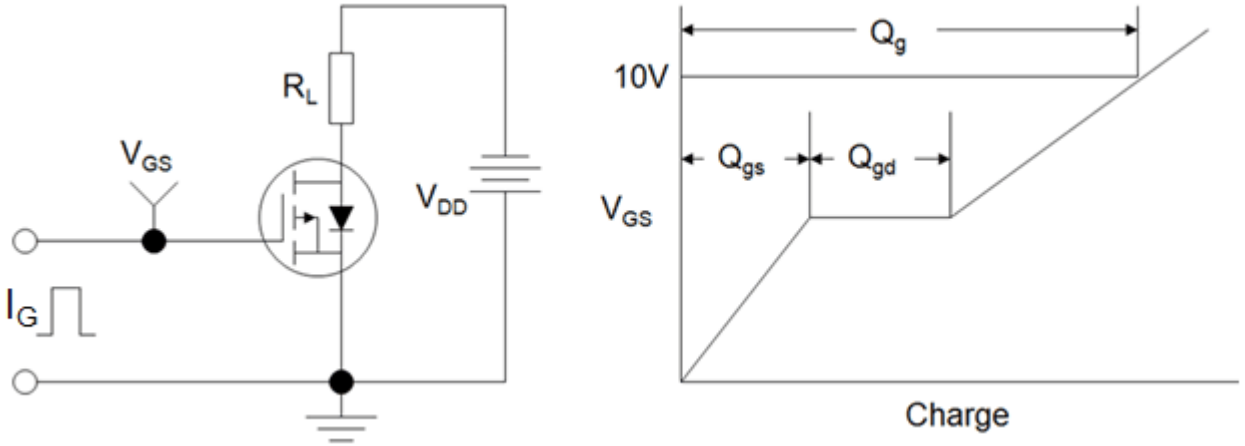
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient (note3)	R_{thJA}	95	ºC/W

Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.5	-0.9	-1.1	V
Drain-Source On-Resistance (note2)	$R_{DS(on)}$	V_{GS} = -10V, I_D = -1A	--	17	20.5	mΩ
		V_{GS} = -4.5V, I_D = -1A	--	21	26	
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-2A	--	10	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz	--	1900	--	pF
Output Capacitance	C_{oss}		--	230	--	
Reverse Transfer Capacitance	C_{rss}		--	150	--	
Total Gate Charge	Q_g	V_{DD} = -15V, I_D = -4A, V_{GS} = -4.5V	--	19	--	nC
Gate-Source Charge	Q_{gs}		--	4	--	
Gate-Drain Charge	Q_{gd}		--	6	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -15V, I_D = -4A, R_G = 6Ω	--	14	--	ns
Turn-on Rise Time	t_r		--	6	--	
Turn-off Delay Time	$t_{d(off)}$		--	60	--	
Turn-off Fall Time	t_f		--	24	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-7	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -1A, V_{GS} = 0V	--	--	-1.2	V

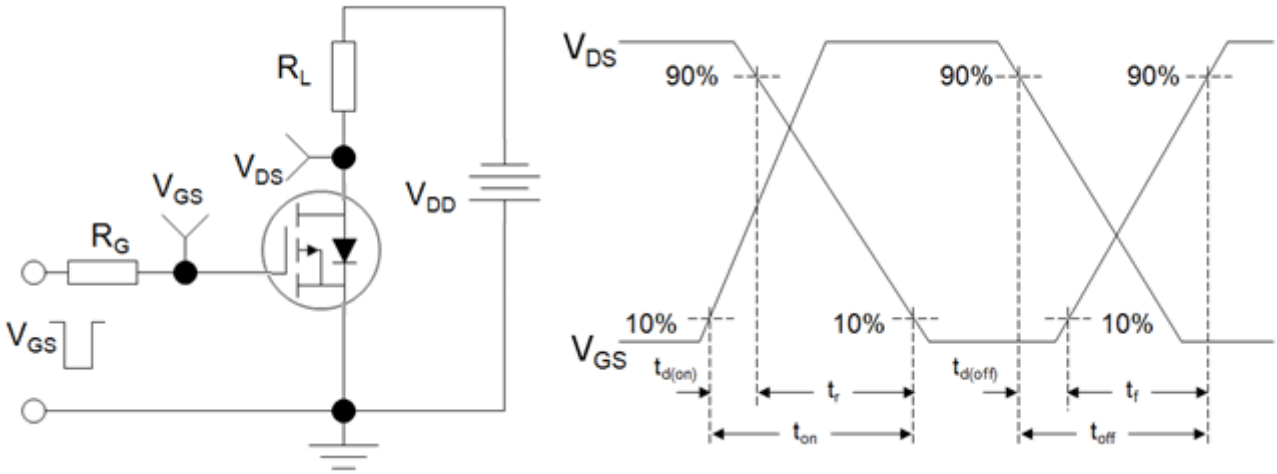
Notes

1.Pulse width limited by Max. junction temperature.
2.Pulse test
3.Surface mounted on 1 in^2 copper pad of FR4 board

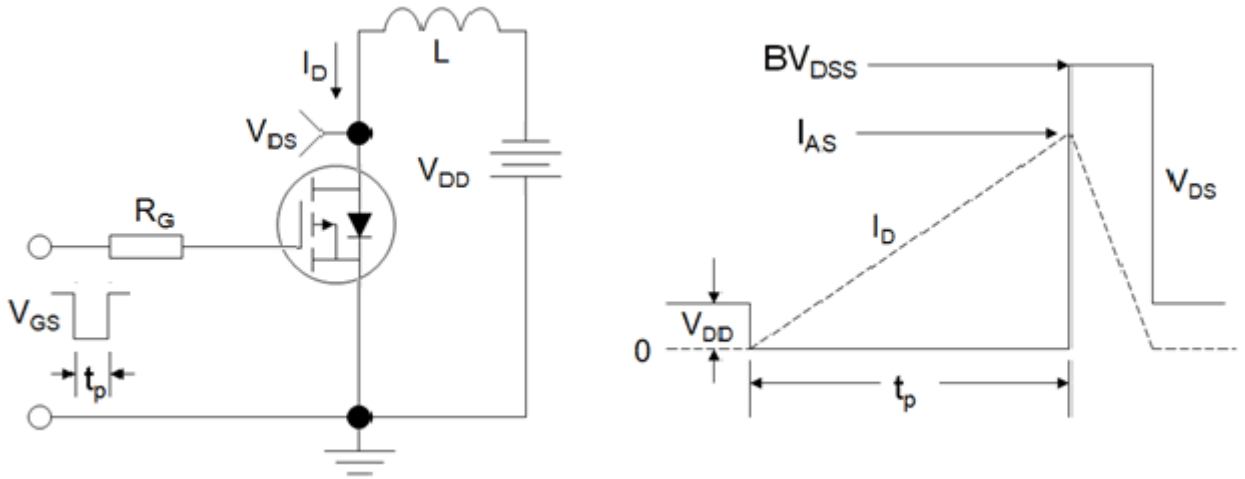
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

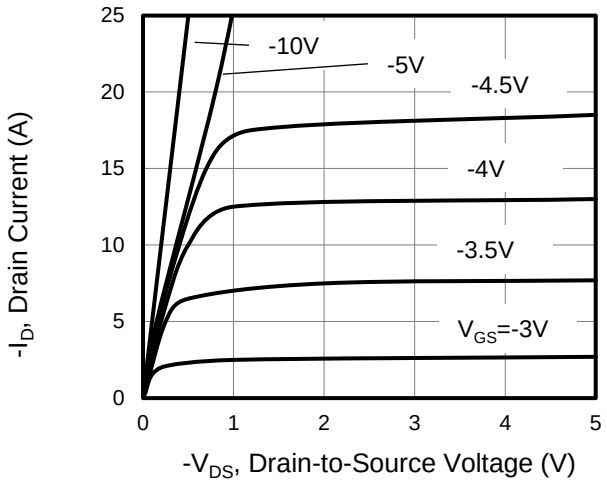


Figure 2. Transfer Characteristics

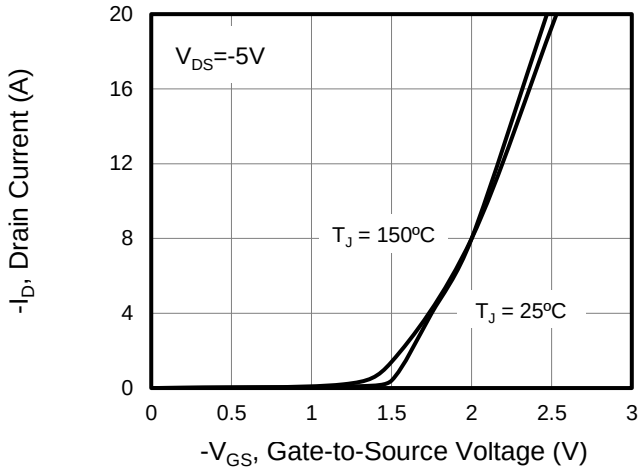


Figure 3. Drain Source On Resistance

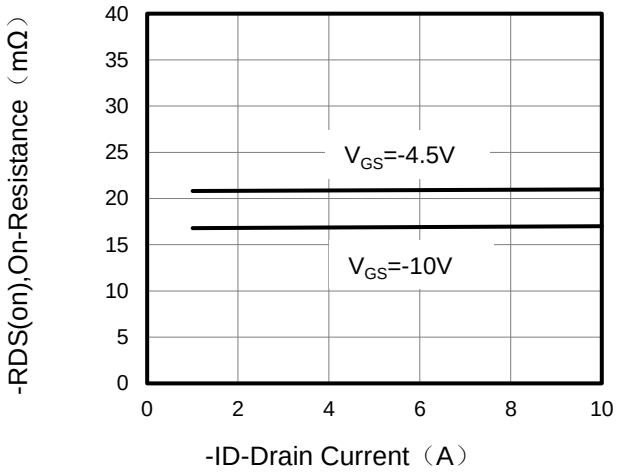


Figure 4. Gate Charge

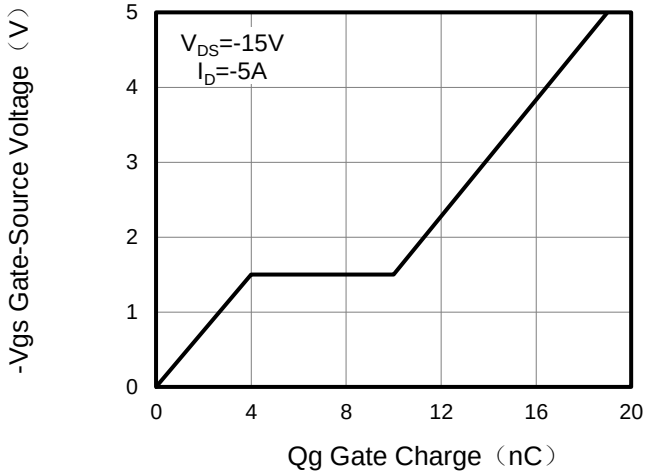


Figure 5. Capacitance vs Vds

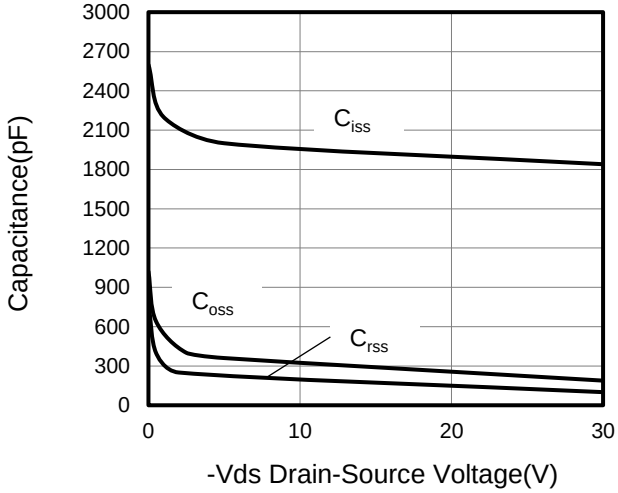
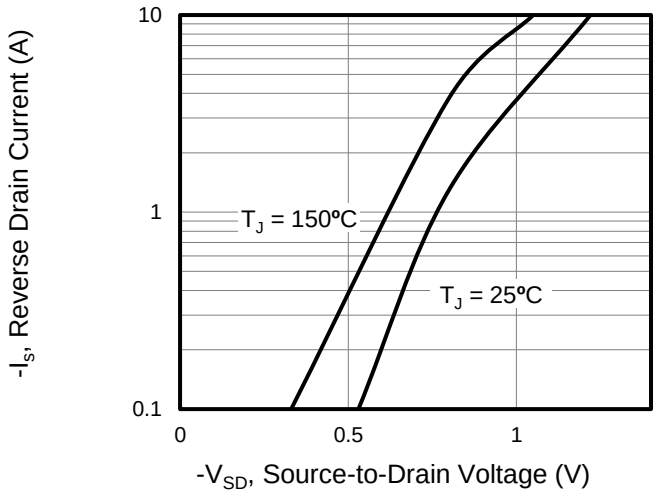


Figure 6. Source-Drain Diode Forward



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

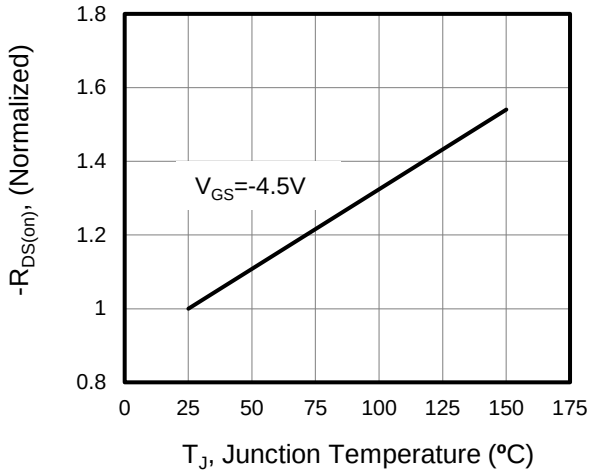


Figure 8. Safe Operation Area

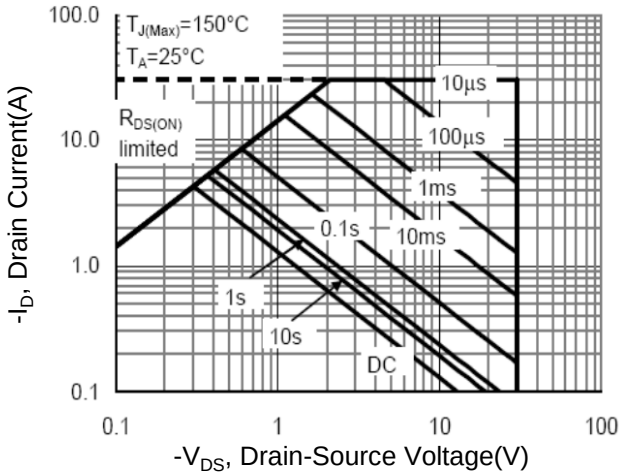
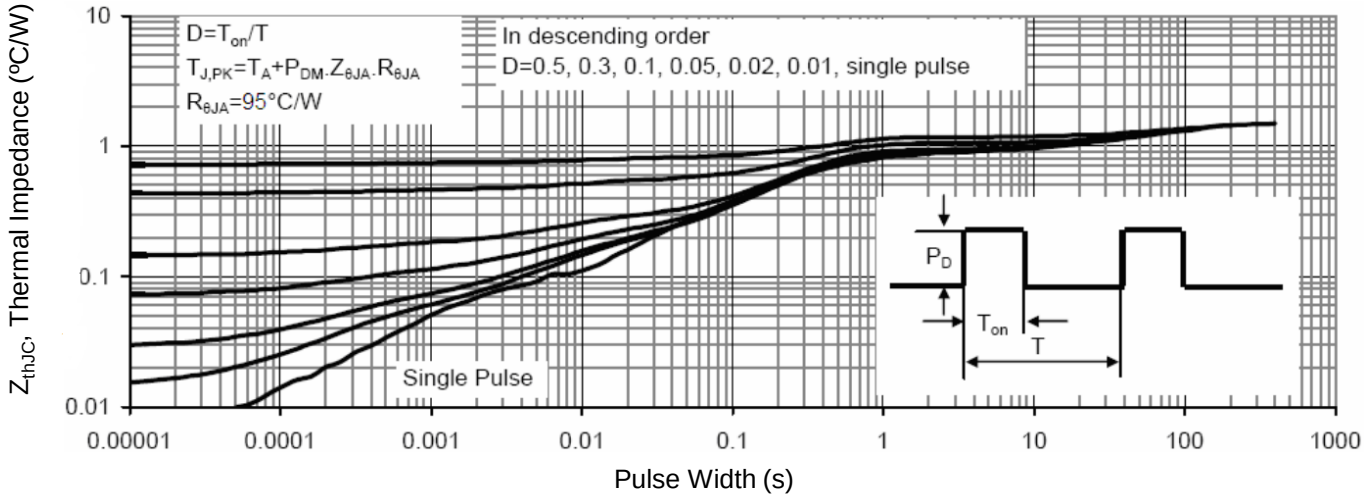
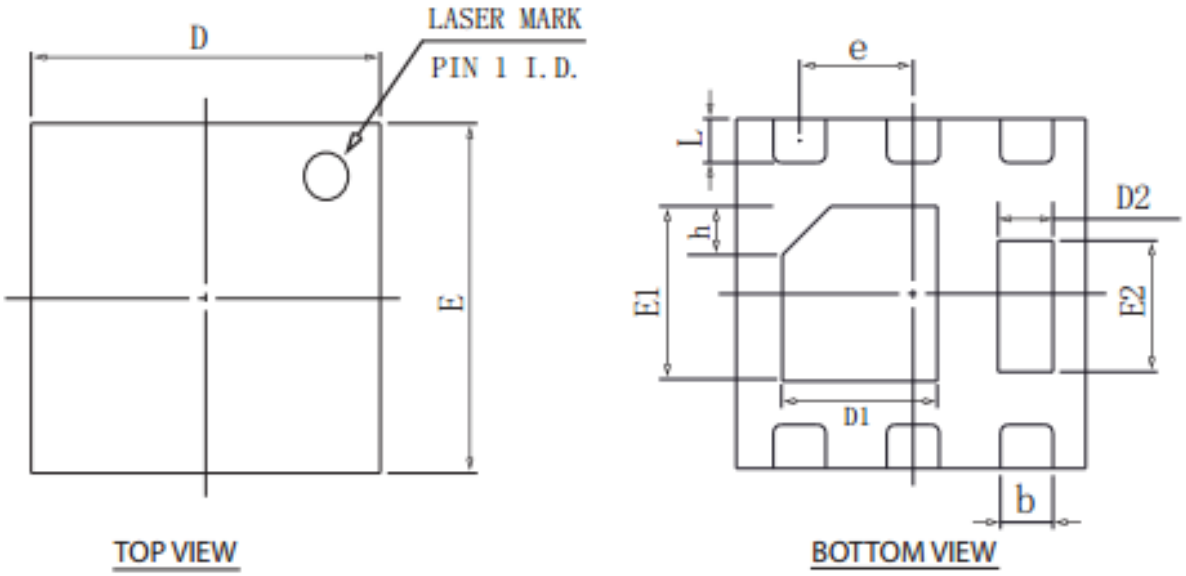
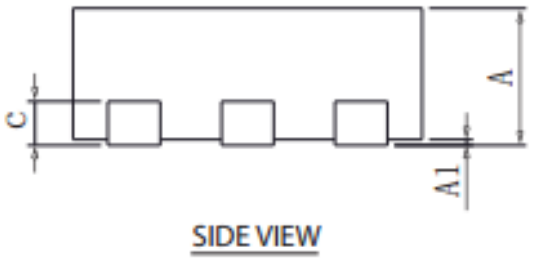


Figure 9. Normalized Maximum Transient Thermal Impedance



DFN2×2-6L Package Information





COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	NA	0.02	0.05
b	0.20	0.27	0.34
c	0.18	0.20	0.25
D	1.95	2.00	2.07
E	1.95	2.00	2.07
D1	0.80	0.90	1.00
E1	0.90	1.00	1.10
D2	0.20	0.30	0.40
E2	0.65	0.75	0.85
L	0.20	0.25	0.35
h	0.20	0.25	0.30
e	0.65BSC		