Description

- Trench Power MV MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- Optimized for fast-switching applications

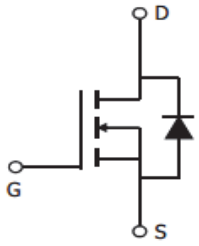
General Features

V_{DSS}	$R_{DS(ON)}$ @4.5V(Typ)	$R_{DS(ON)}$ @10V(Typ)	I_D
100V	8.9 mΩ	6.6 mΩ	15A

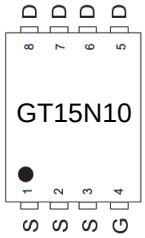
- High power and current handing capability
- RoHS Compliant
- Surface mount package

Applications

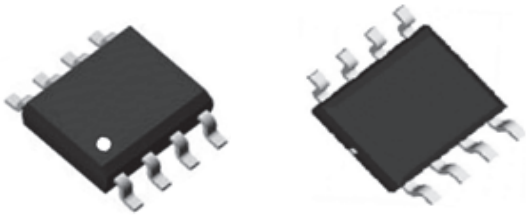
- Synchronus Rectification in DC/DC and AC/DC Converters
- Industrial and Motor Drive applications



Schematic diagram



Marking and pin assignment



SOP-8

Ordering Information

Part Number	Marking	Case	Packaging
GT15N10	GT15N10	SOP-8	4000pcs/Reel

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current G	T_A=25°C	I_D	15	A
	T_A=100°C		9.5	
Pulsed Drain Current C		I_{DM}	55	A
Avalanche energy L=0.3mH C		E_{AS}	150	mJ
Power Dissipation A	T_A=25°C	P_{DSM}	3.1	W
	T_A=70°C		2.0	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Maximum		Units
Maximum Junction-to-Ambient A	t ≤ 10s	$R_{\theta JA}$	30	40	°C/W
Maximum Junction-to-Ambient A D	Steady-State		58	75	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	15	24	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.3	1.9	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=7.5A		6.6	7.8	mΩ
		T_J=125°C		11.6	13.7	
		V_{GS}=4.5V, I_D=7.5A		8.9	10.5	
g_{FS}	Diode Forward Voltage	V_{DS}=5V, I_D=7.5A	30			S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	0.95	V
I_S	Maximum Body-Diode Continuous Current [G]				48	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		2808		pF
C_{oss}	Output Capacitance			961		pF
C_{rss}	Reverse Transfer Capacitance			23		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=50V, I_D=7.5A		50		nC
Q_g(4.5V)	Total Gate Charge			33		nC
Q_{gs}	Gate Source Charge			17		nC
Q_{gd}	Gate Drain Charge			11		nC
$t_{D(on)}$	Turn-on Delay Time	V_{GS}=10V, V_{DS}=50V, R_L=2.5Ω, R_{GEN}=3Ω		15		ns
t_r	Turn-on Rise Time			12		ns
$t_{D(off)}$	Turn-off Delay Time			25		ns
t_f	Turn-off Fall Time			13		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=15A,di/dt=500A/μs		45		ns
Q_{rr}	Body Diode Reverse Recovery charge	I_F=15A,di/dt=500A/μs		140		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature TJ(MAX)=150° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

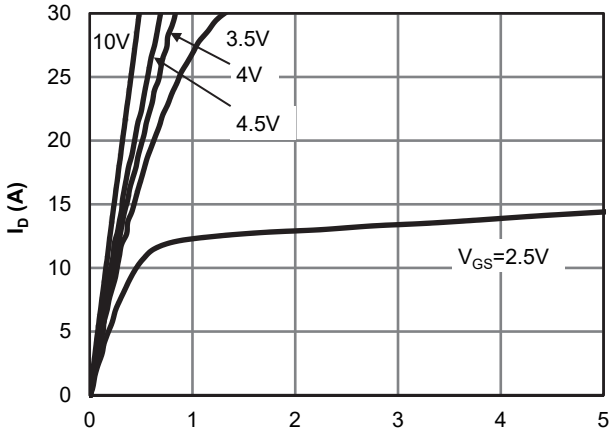


Fig 1: On-Region Characteristics

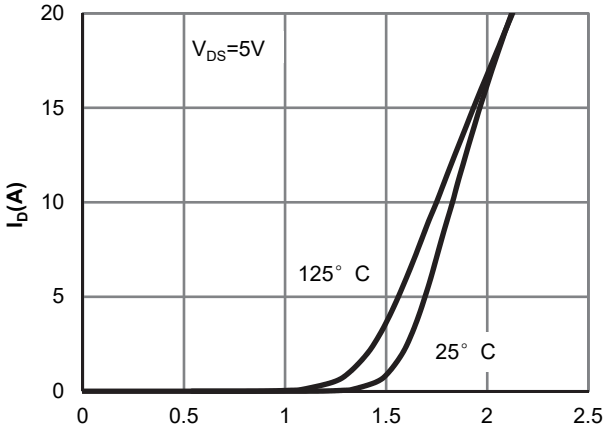


Figure 2: Transfer Characteristics

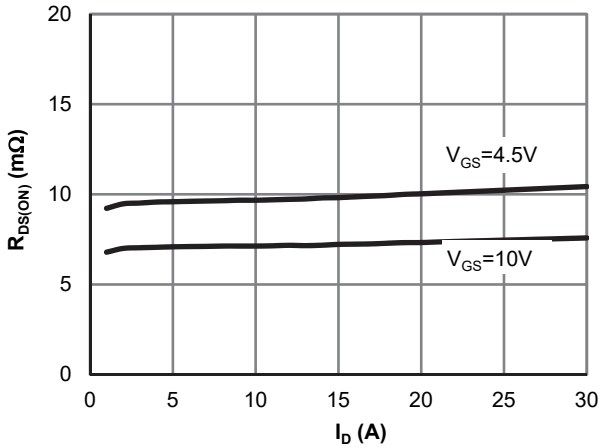


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

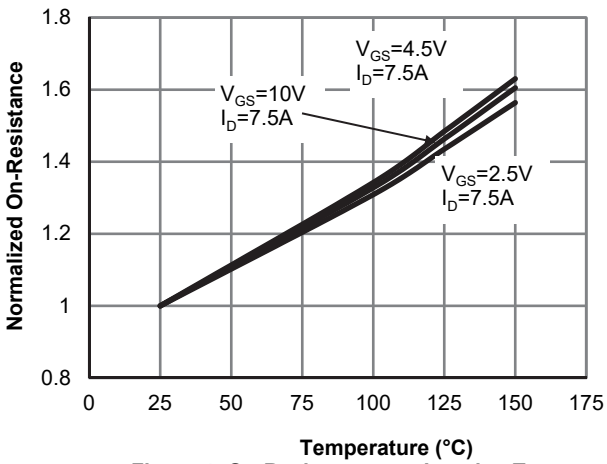


Figure 4: On-Resistance vs. Junction Temperature

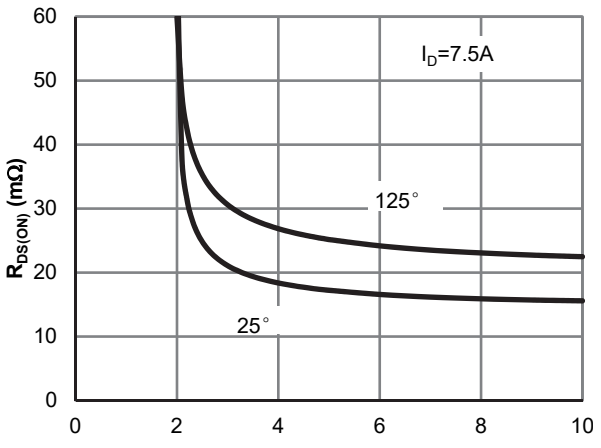


Figure 5: On-Resistance vs. Gate-Source Voltag

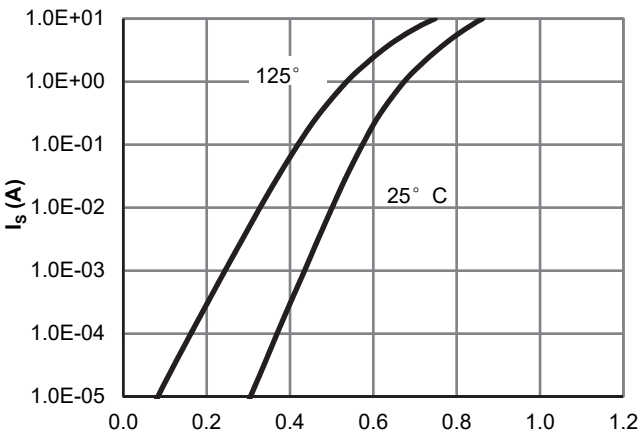


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

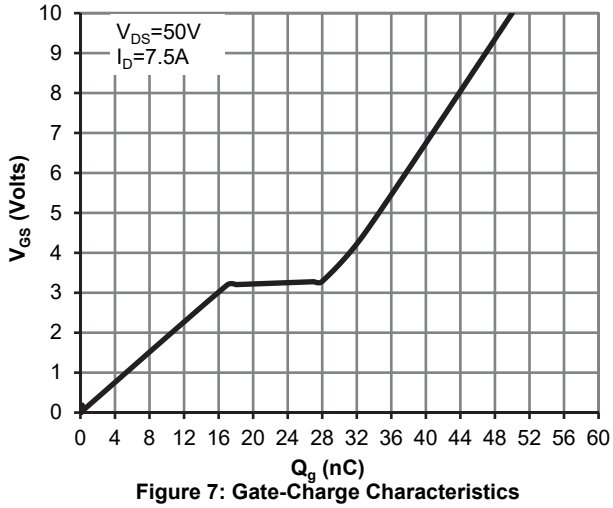


Figure 7: Gate-Charge Characteristics

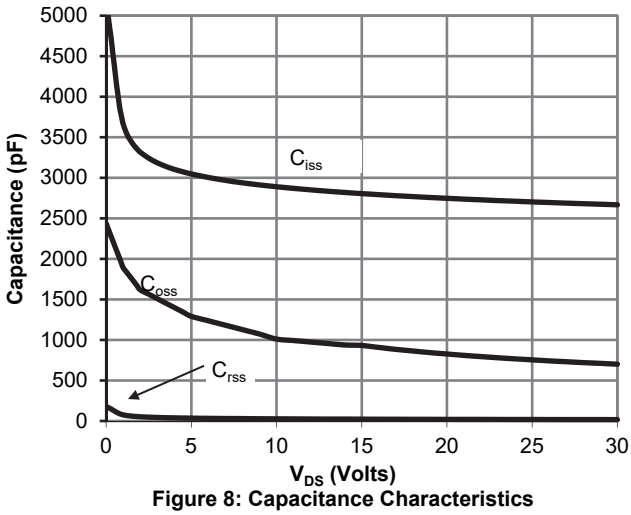
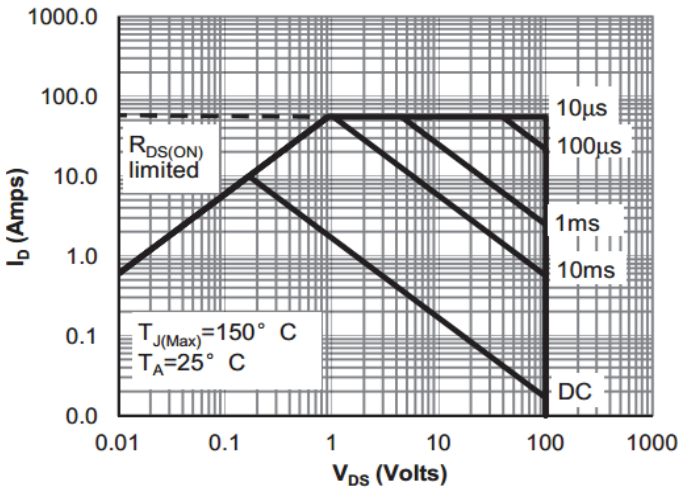


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

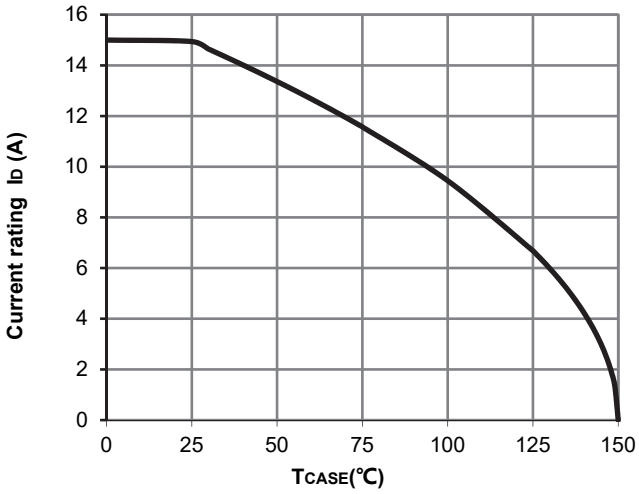


Figure 10: Current De-rating (Note F)

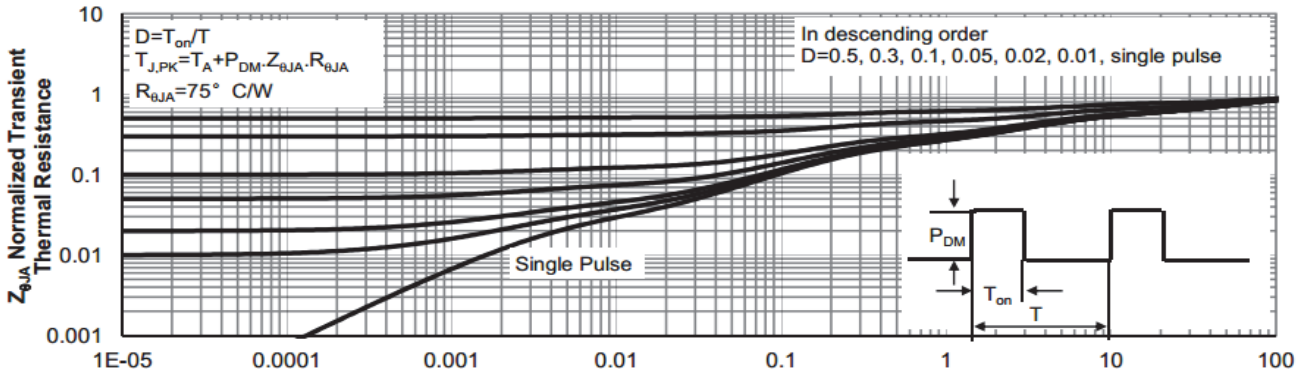


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Figure A: Gate Charge Test Circuit & Waveforms

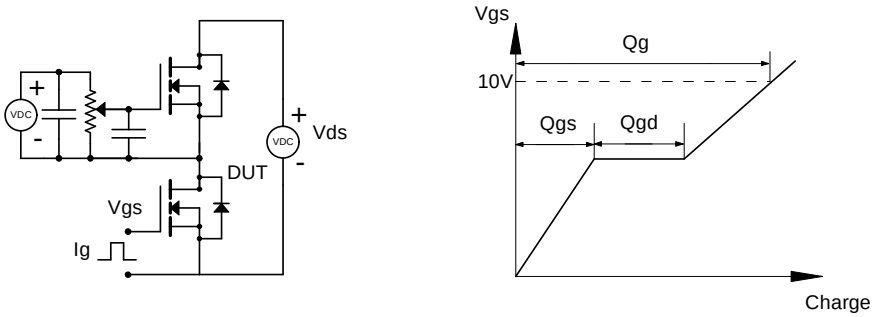


Figure B: Resistive Switching Test Circuit & Waveforms

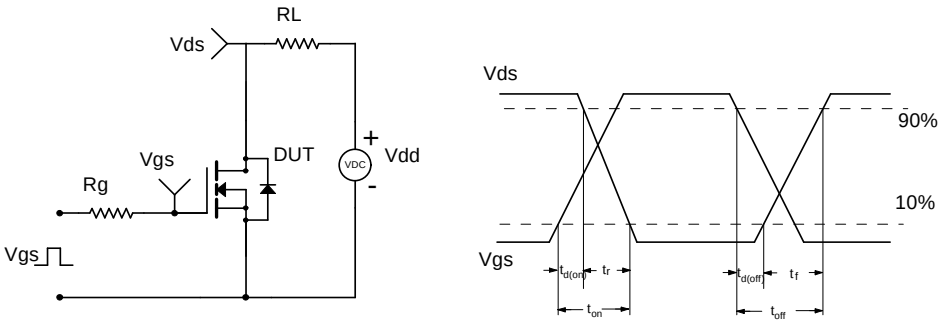


Figure C: Unclamped Inductive Switching (UIS) Test

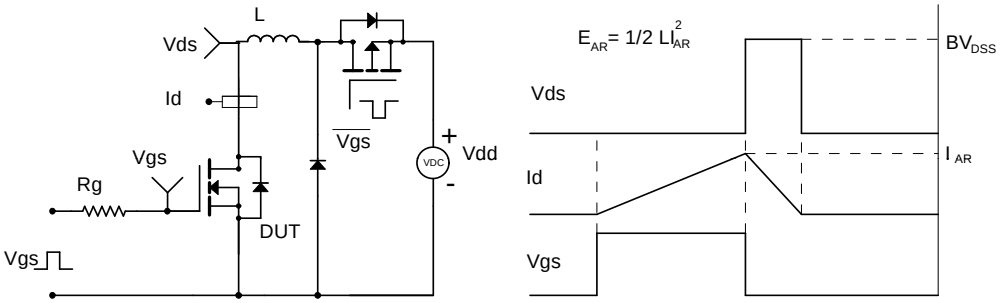
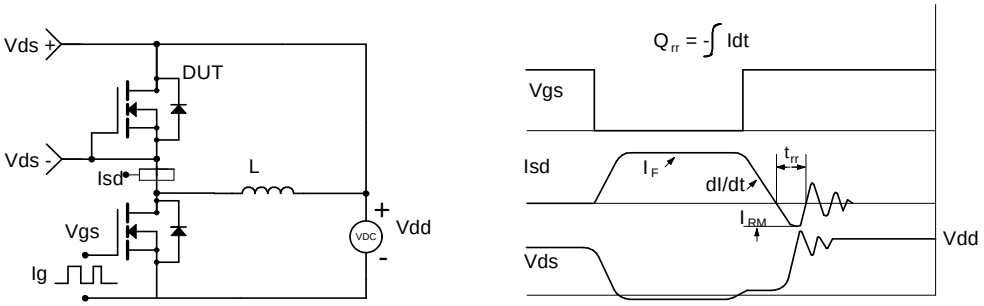
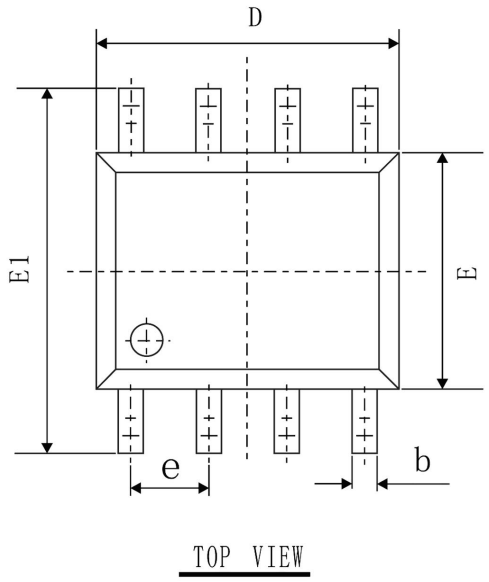


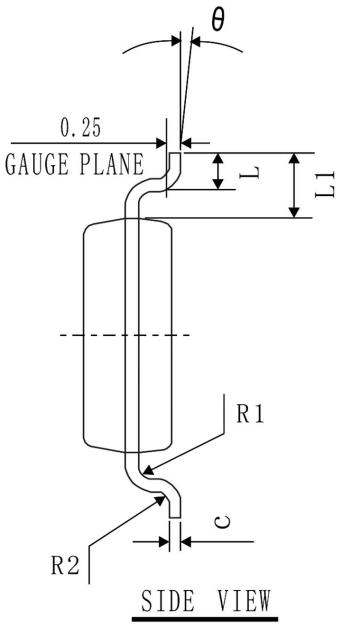
Figure D: Diode Recovery Test Circuit & Waveforms



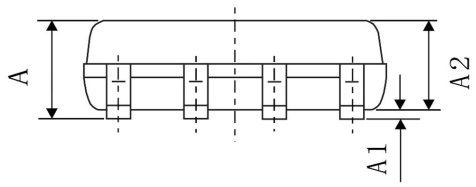
SOP-8 Package information



TOP VIEW



SIDE VIEW



SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	1.40	1.60	1.80
A1	0.05	0.15	0.25
A2	1.35	1.45	1.55
b	0.30	0.40	0.50
c	0.153	0.203	0.253
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
L	0.45	0.70	1.00
θ	2°	4°	6°
L1	1.04 REF		
e	1.27 BSC		
R1	0.07 TYP		
R2	0.07 TYP		