P-Channel Enhancement Mode Power MOSFET

Description

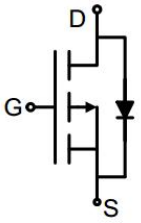
The GT750P10D5 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

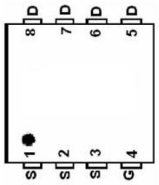
- V_{DS} -100V
- I_D (at V_{GS} = -10V) -24A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 60mΩ
- $R_{DS(ON)}$ (at V_{GS} = -4.5V) < 75mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

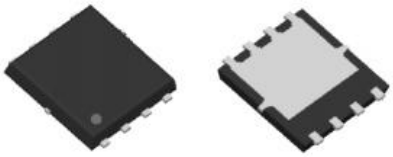
- Power switch
- DC/DC converters



Schematic diagram



pin assignment



DFN5X6-8L

Ordering Information

Device	Package	Marking	Packaging
GT750P10D5	DFN5X6-8L	GT750P10	5000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-100	V
Continuous Drain Current	T_C = 25ºC	I_D	-24	A
	T_C = 100ºC		-15	
Pulsed Drain Current (note1)		I_{DM}	-96	A
Gate-Source Voltage		V_{GS}	±20	V
Power Dissipation		P_D	79	W
Single pulse avalanche energy （note2）		E_{AS}	81	mJ
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 To 150	ºC

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	ºC/W
Maximum Junction-to-Case	R_{thJC}	1.58	ºC/W

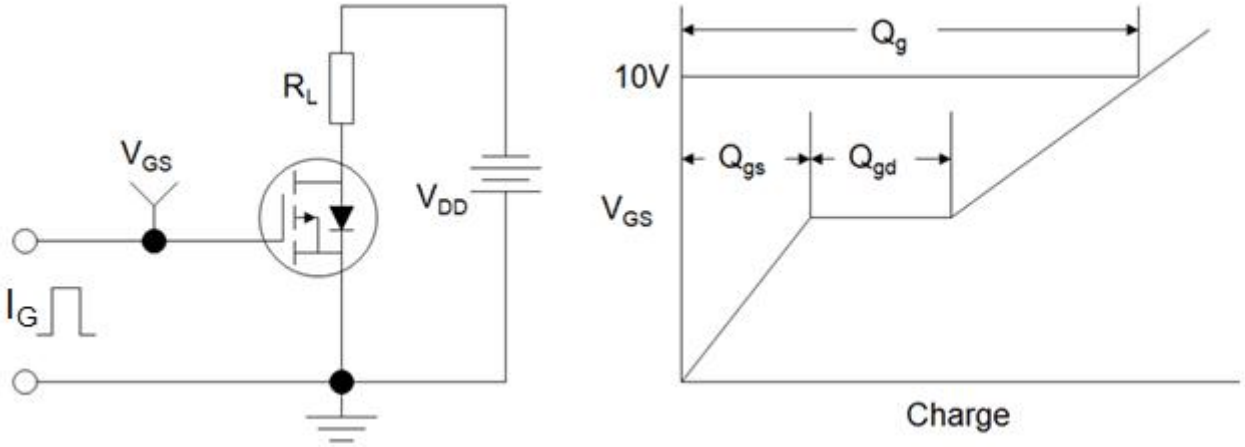
Specifications T_J = 25ºC, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100V, V_{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-1.8	-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -10A	--	50	60	mΩ
		V_{GS} = -4.5V, I_D = -10A	--	62	75	
Forward Transconductance	g_{FS}	V_{DS} = -5V,I_D = -10A	--	22	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -50V, f = 1.0MHz	--	1950	--	pF
Output Capacitance	C_{oss}		--	155	--	
Reverse Transfer Capacitance	C_{rss}		--	20	--	
Total Gate Charge	Q_g	V_{DD} = -50V, I_D = -10A, V_{GS} = -10V	--	29	--	nC
Gate-Source Charge	Q_{gs}		--	5	--	
Gate-Drain Charge	Q_{gd}		--	3	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -50V, I_D = -10A, R_G = 6Ω	--	13	--	ns
Turn-on Rise Time	t_r		--	39	--	
Turn-off Delay Time	$t_{d(off)}$		--	100	--	
Turn-off Fall Time	t_f		--	105	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-24	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -10A, V_{GS} = 0V	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	I_F = -10A, V_{GS} = 0V di/dt=-100A/us	--	280	--	nC
Reverse Recovery Time	T_{rr}		--	104	--	ns

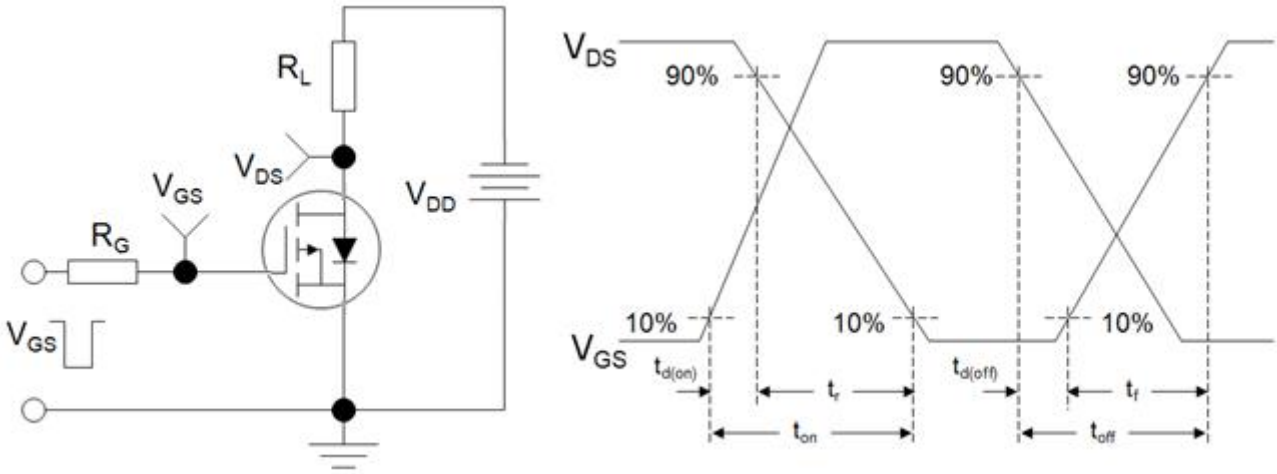
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=50V,VGS=10V,L=0.5mH,Rg=25Ω
   The table shows the minimum avalanche energy, which is 225mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

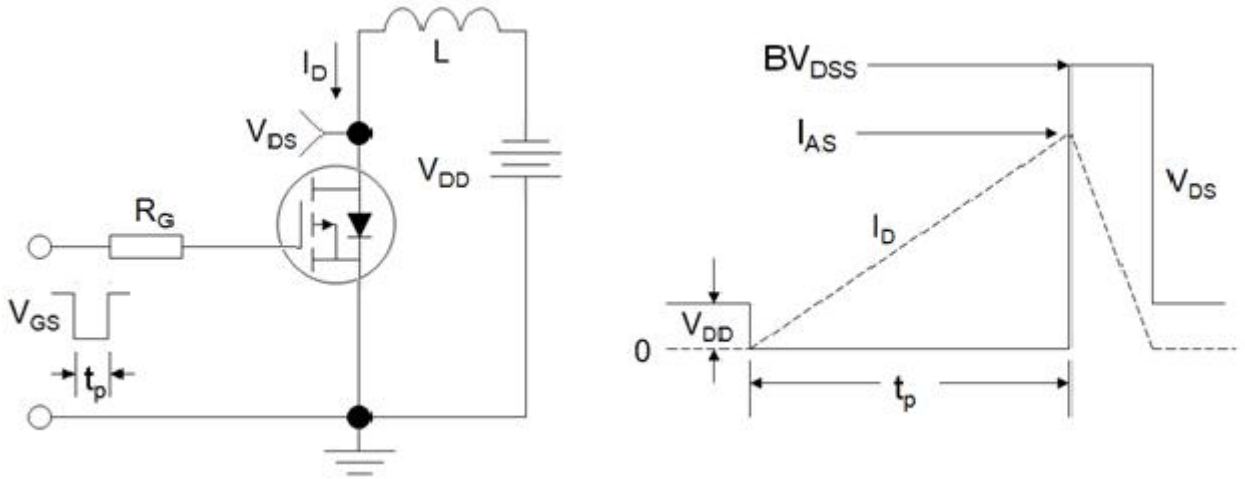
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

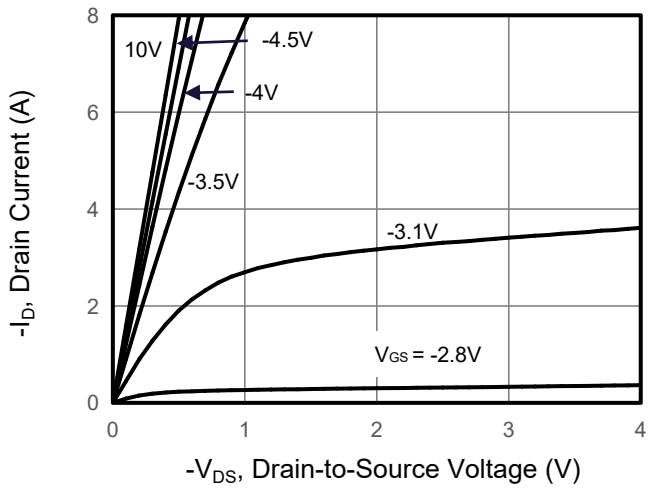


Figure 2. Transfer Characteristics

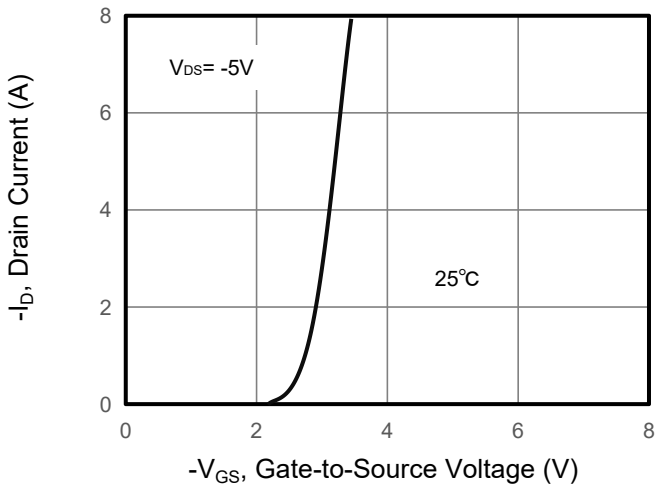


Figure 3.Drain Source On Resistance

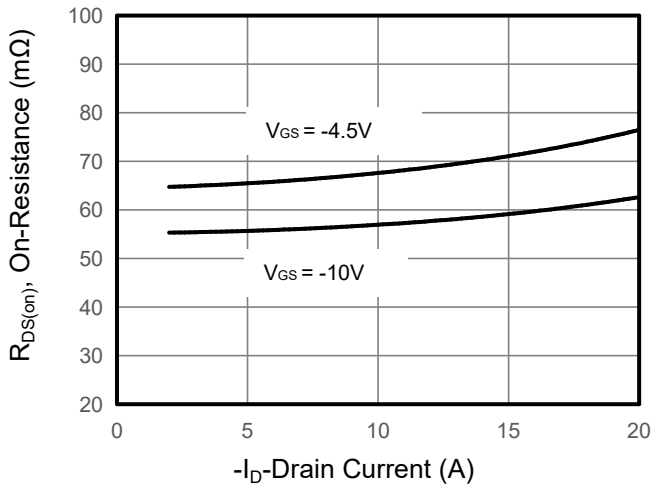


Figure 4. Gate Charge

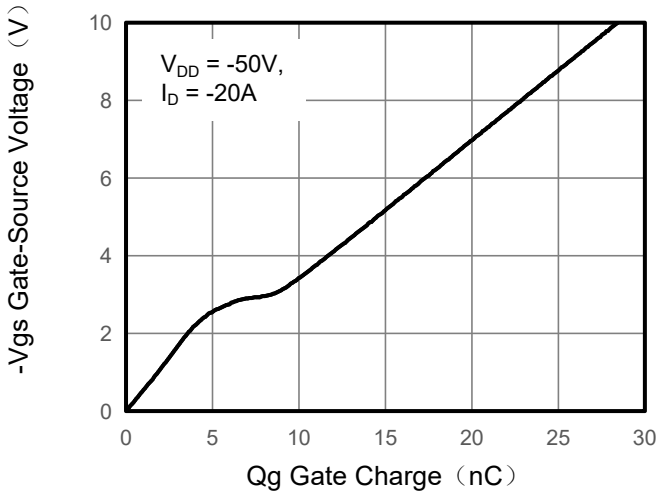


Figure 5. Capacitance

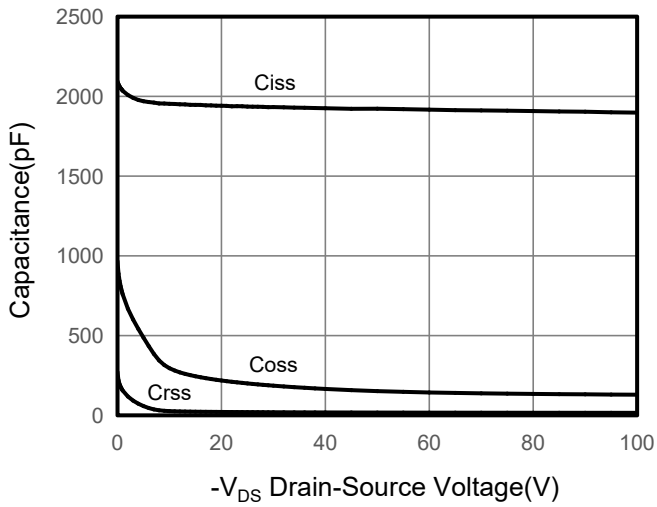
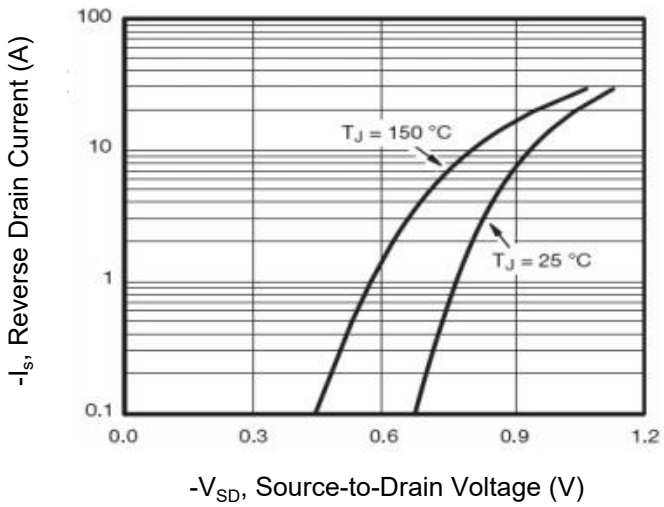


Figure 6. Source-Drain Diode Forward



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

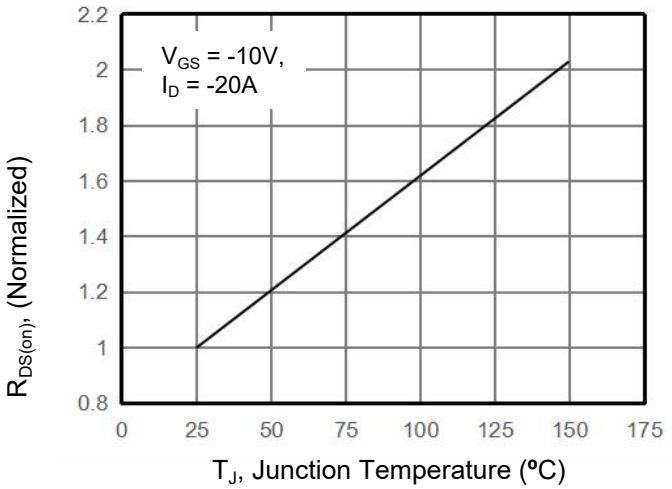


Figure 8. Safe Operation Area

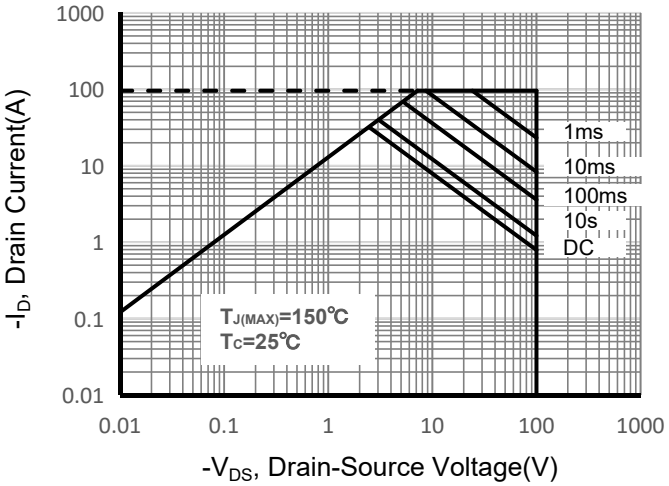


Figure 9. Maximum Continuous Drain Current vs Case Temperature

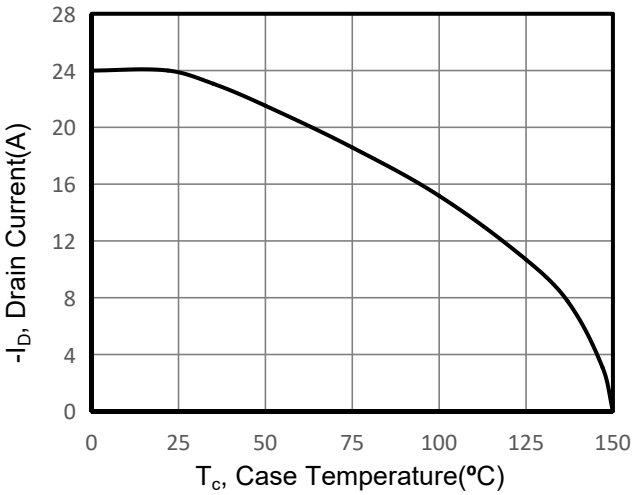
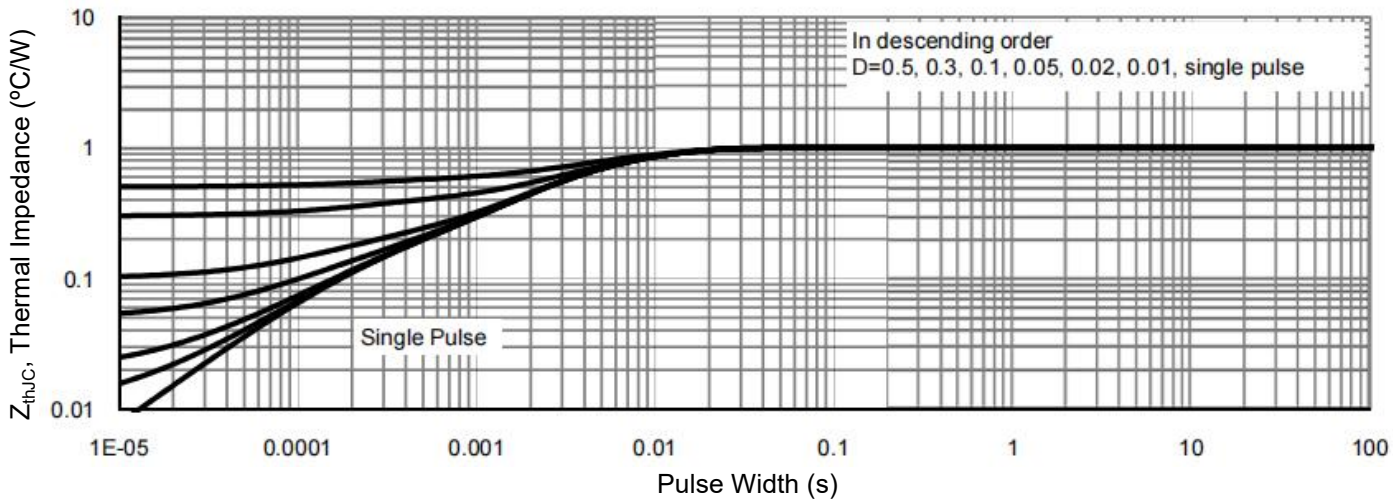
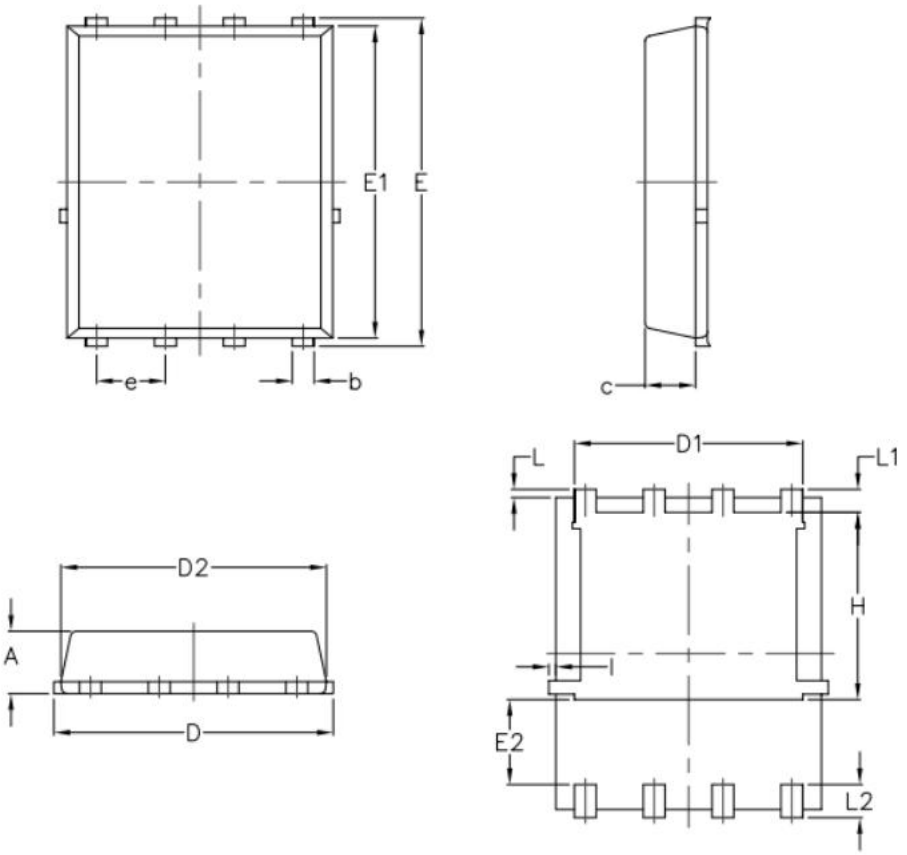


Figure 10. Normalized Maximum Transient Thermal Impedance



DFN5X6-8L Package Information



	SYMBOL	COMMON			
		MM		INCH	
		MIN.	MAX.	MIN.	MAX.
	A	1.03	1.17	0.0406	0.0461
	b	0.34	0.48	0.0134	0.0189
	c	0.824	0.970	0.0324	0.0382
3	D	4.80	5.40	0.1890	0.2126
	D1	4.11	4.31	0.1618	0.1697
3	D2	4.80	5.00	0.1890	0.1969
	E	5.95	6.15	0.2343	0.2421
	E1	5.65	5.85	0.2224	0.2303
5	E2	1.40	—	0.0551	—
	e	1.27 BSC		0.05 BSC	
3	L	0.05	0.25	0.0020	0.0098
	L1	0.38	0.50	0.0150	0.0197
5	L2	0.38	0.71	0.0150	0.0280
4	H	3.30	3.50	0.1299	0.1378
	I	—	0.18	—	0.0070