N-Channel 800V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	800	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	1.2
Q_g (Max.) (nC)	200	
Q_{gs} (nC)	24	
Q_{gd} (nC)	110	
Configuration	Single	

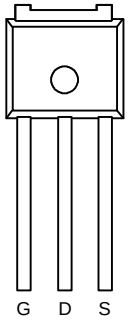
FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

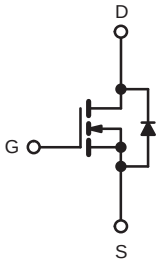
Available

RoHS* COMPLIANT

TO-251



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	800	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	5	A
		T_C = 100 °C		3.9	
Pulsed Drain Current[a]			I_{DM}	21	
Linear Derating Factor				1.5	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	770	mJ
Repetitive Avalanche Current[a]			I_{AR}	7.8	A
Repetitive Avalanche Energy[a]			E_{AR}	19	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	190	W
Peak Diode Recovery dV/dt[c]			dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 23 mH, R_g = 25 Ω, I_{AS} = 7.8 A (see fig. 12).
c. I_{SD} ≤ 7.8 A, dI/dt ≤ 140 A/μs, V_{DD} ≤ 600 V, T_J ≤ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.65	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		800	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.98	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 800 V, V_{GS} = 0 V		-	-	100	µA
		V_{DS} = 640 V, V_{GS} = 0 V, T_J = 125 °C		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 3.7 A[b]	–	1.2	-	Ω
Forward Transconductance	g_{fs}	V_{DS} = 100 V, I_D = 3.7 A[b]		5.6	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	3100	-	pF
Output Capacitance	C_{oss}			-	800	-	
Reverse Transfer Capacitance	C_{rss}			-	490	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 3.8 A, V_{DS} = 400 V, see fig. 6 and 13[b]	-	-	200	nC
Gate-Source Charge	Q_{gs}			-	-	24	
Gate-Drain Charge	Q_{gd}			-	-	110	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 3.8 A, R_g = 6.2 Ω, R_D= 52 Ω see fig. 10[b]		-	19	-	ns
Rise Time	t_r			-	38	-	
Turn-Off Delay Time	$t_{d(off)}$			-	120	-	
Fall Time	t_f			-	39	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	5.0	-	nH
Internal Source Inductance	L_S			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5.0	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	21	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 3.8 A, V_{GS} = 0 V[b]		-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 3.8 A, dI/dt = 100 A/µs[b]		-	650	980	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.8	5.7	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

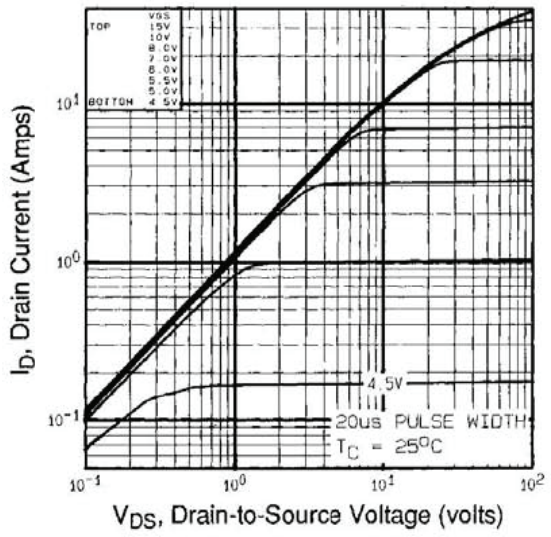


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

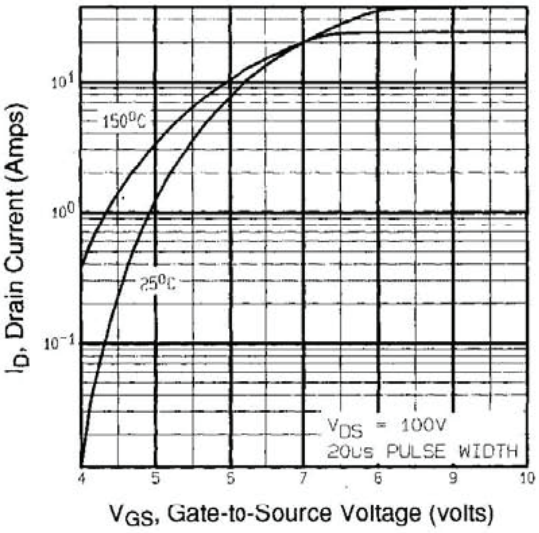


Fig. 3 - Typical Transfer Characteristics

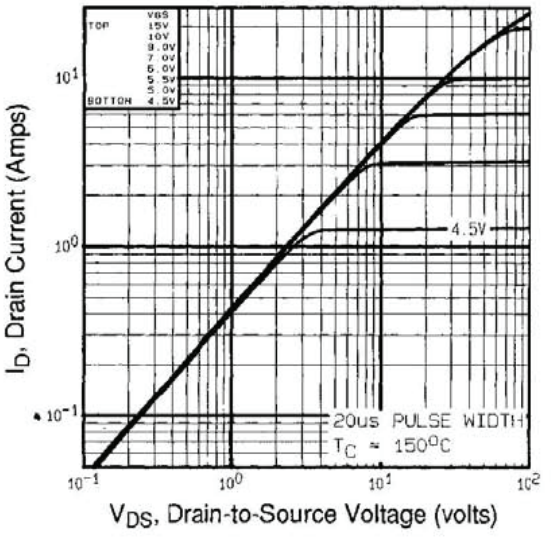


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

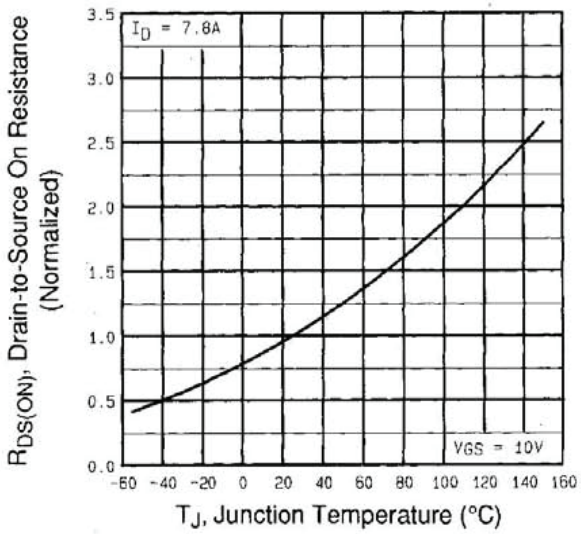


Fig. 4 - Normalized On-Resistance vs. Temperature

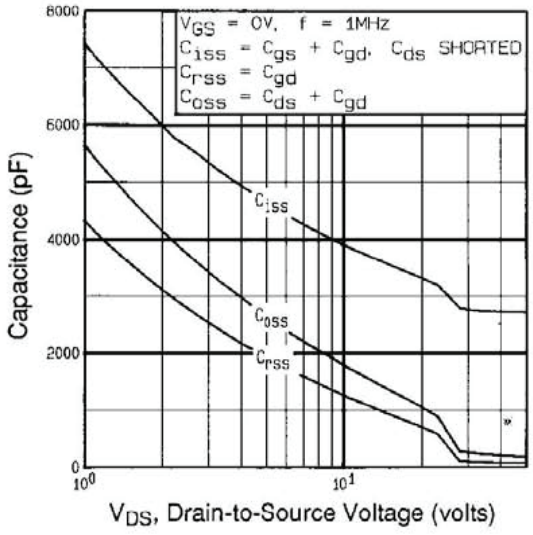


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

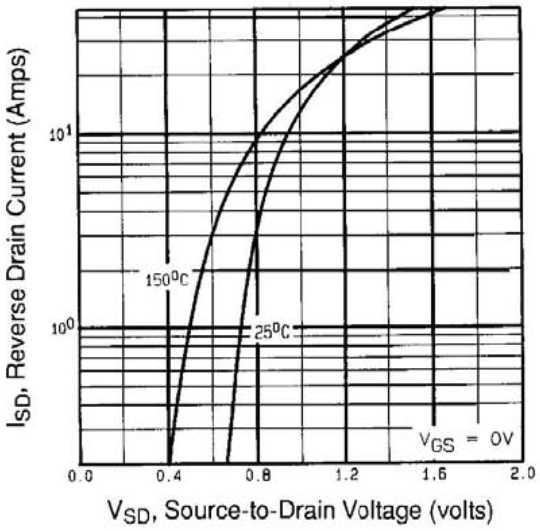


Fig. 7 - Typical Source-Drain Diode Forward Voltage

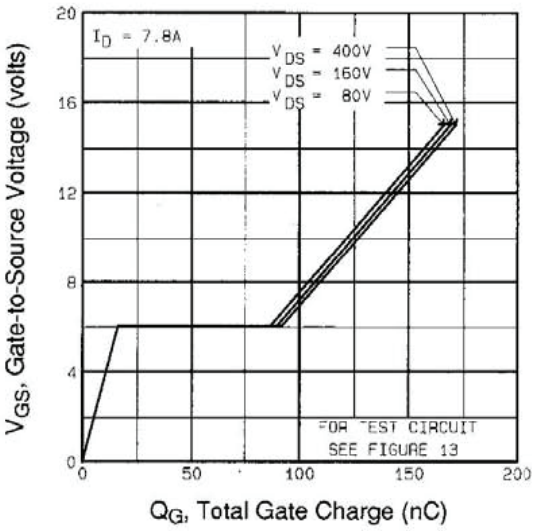


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

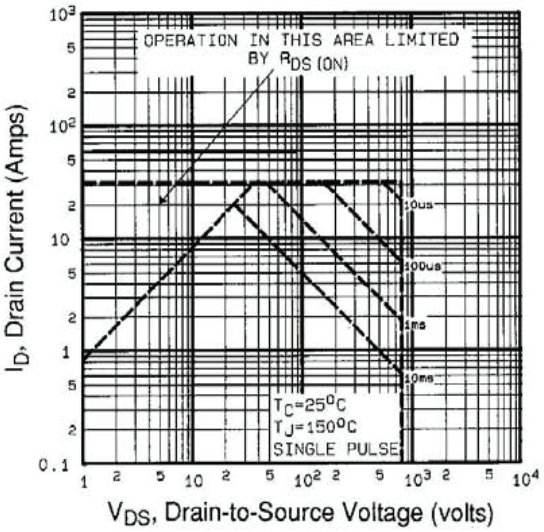


Fig. 8 - Maximum Safe Operating Area

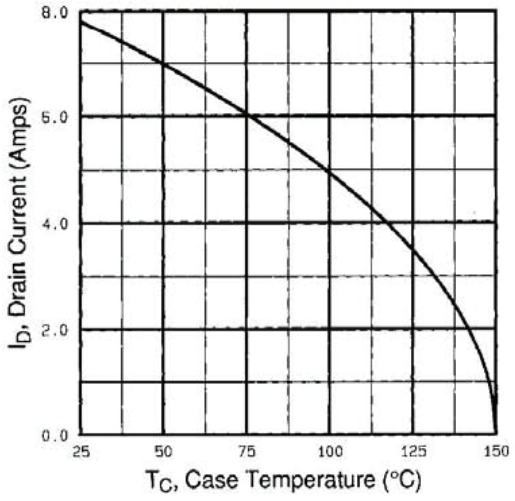


Fig. 9 - Maximum Drain Current vs. Case Temperature

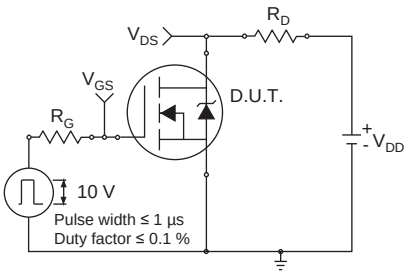


Fig. 10a - Switching Time Test Circuit

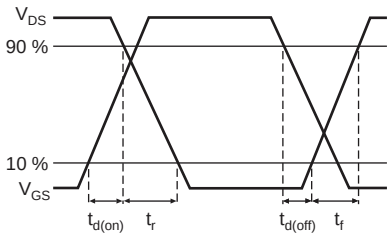


Fig. 10b - Switching Time Waveforms

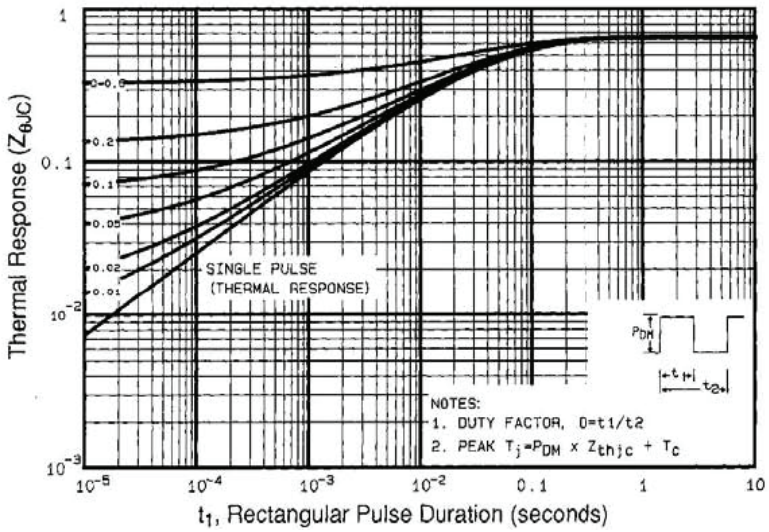


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

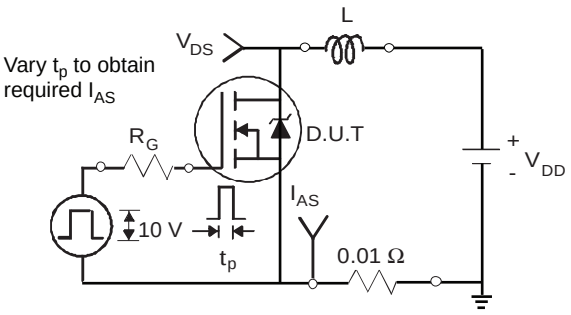


Fig. 12a - Unclamped Inductive Test Circuit

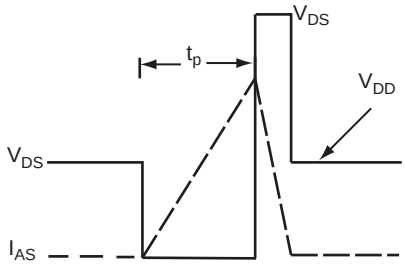


Fig. 12b - Unclamped Inductive Waveforms

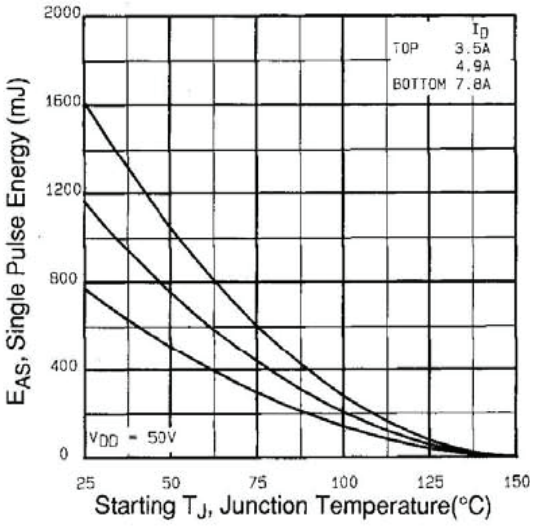


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

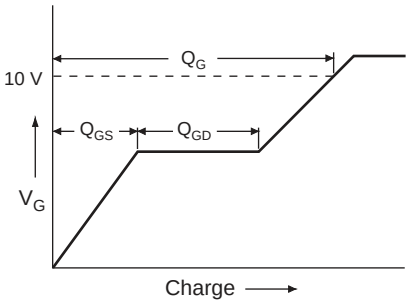


Fig. 13a - Basic Gate Charge Waveform

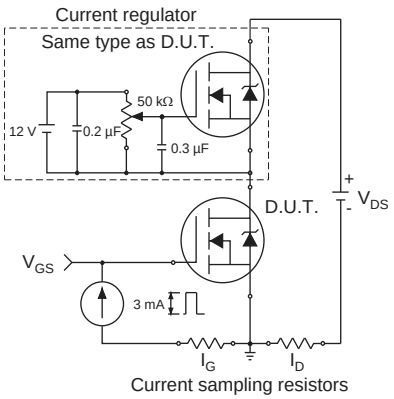
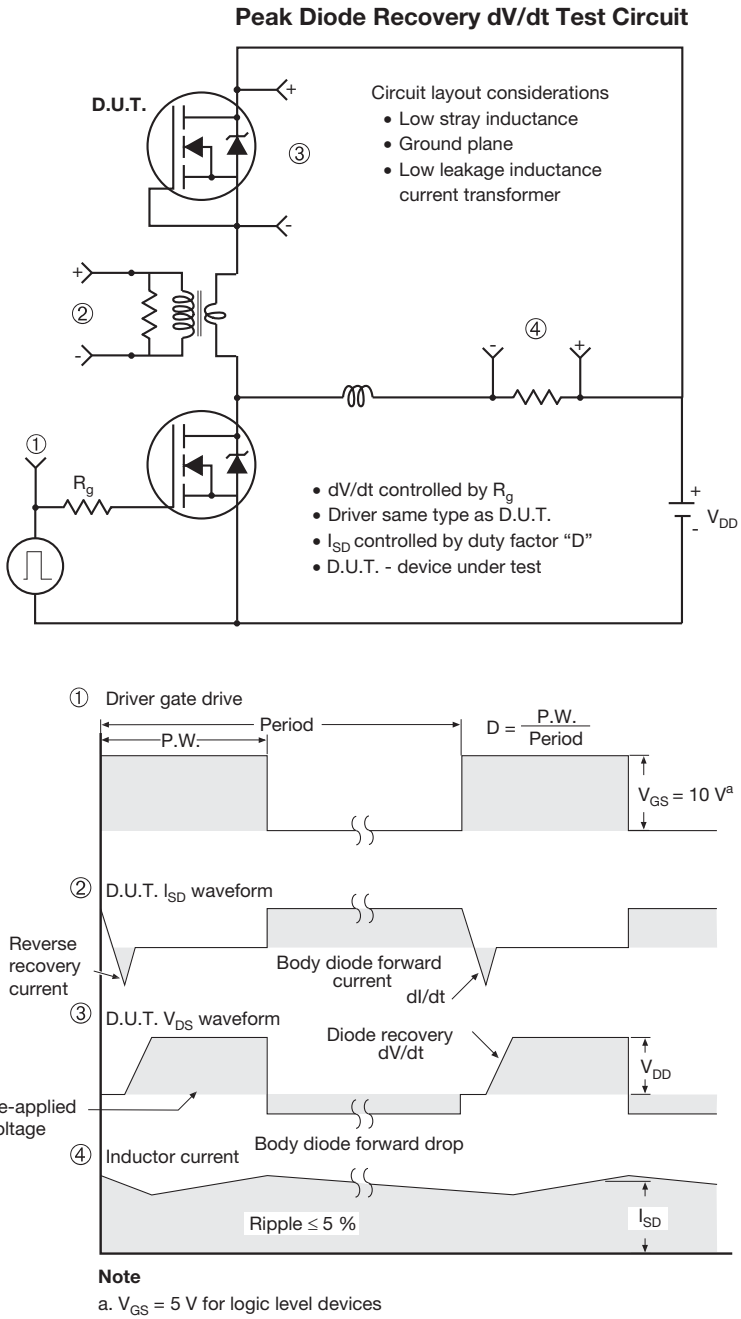


Fig. 13b - Gate Charge Test Circuit

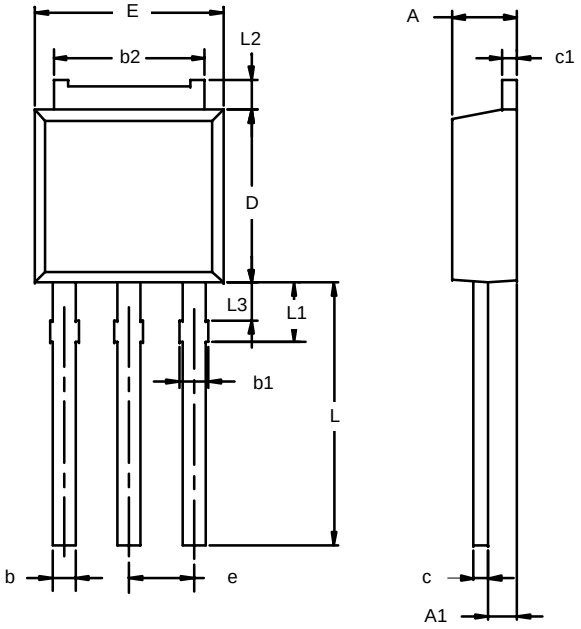


Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

TO-251AA (DPAK)



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
b	0.71	0.89	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.43	0.206	0.214
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
E	6.48	6.73	0.255	0.265
e	2.28 BSC		0.090 BSC	
L	3.89	9.53	0.153	0.375
L1	1.91	2.28	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.045	0.060
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5346				

Note: Dimension L3 is for reference only.

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